X-ray Diffraction Residual Stress Measurement at Room Temperature and 77 K in a Microelectronic Multi-layered Single-Crystal Structure Used for Infrared Detection

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The electronic assembly considered in this study is an infrared (IR) detector consisting of different layers, including (111) CdHgTe and (100) silicon single crystals. The processing steps and the low working temperature (77 K) induce thermomechanical stresses that can affect the reliability of the thin and brittle CdHgTe detection circuit and lead to failure. These residual stresses have been quantified in both CdHgTe and silicon circuits at room temperature (293 K) and cryogenic temperature using x-ray diffraction. A specific experimental device has been developed for 77 K measurements and a method developed for single-crystal analysis has been adapted to such structures using a laboratory four-circle diffractometer. This paper describes the methodology to obtain the deformed lattice parameter and compute the strain/stress tensors. Whereas the stresses in the CdHgTe layer appear to be negative at room temperature (compressive values), cryogenic measurements show a tensile biaxial stress state of about 30 MPa and highlight the great impact of low temperature on the mechanical properties.

Key words: Semiconductor compounds, x-ray diffraction, cryogenic temperature, residual stresses, thermomechanical processing

INTRODUCTION

Nowadays, industrial sectors (health, energy, defence and aerospace) innovations are dependent on the microelectronic industry which has to deal with ever more strenuous requirements in terms of high performance and minimum dimensions. To meet the steadily growing demand, 3D integration is a promising solution. In this architecture, chips of different natures performing various functions in the system are stacked and interconnected vertically. However, extreme thermomechanical stresses are generated during the processing steps and at the working temperature (77 K) due to the multilayer architecture as well as the presence of heterogeneous and brittle materials. Expansion coefficient mismatches, temperature gradients, misalignment and other process factors lead to assembly warpage which can affect the chips' reliability and service life. In addition, stress and strain modify the crystallographic structure of the materials which can deteriorate the electronic functions by a band gap modification of semiconductors.

In this study, a cooled CdHgTe-based infrared (IR) detector architecture is considered. This technology using the properties of CdHgTe is subjected to significant international competition requiring high research efforts in this area. Thus, the current development aims at increasing the pixel density of the detection circuit in order to evolve towards better resolution for large detector applications. Several complications occur in the assembly due to the temperature gradient (ambient to 77 K) as the CdHgTe chip warpage induces residual stresses and can lead to cleavage failure. This issue is mainly due to the difference in mechanical properties and the

high expansion coefficient mismatch between the various layers: the CdHgTe detection circuit can be assimilated to a thin film compared to the silicon substrate.[1] The main motivation of this work is to better understand the apparition of failure in the CdHgTe detection circuit by quantification of the residual stresses induced by the manufacturing process and then upon cooling, because they are known to have a strong impact on the service reliability. A few authors have made some experimental measurements to quantify the strain induced in epitaxy-grown CdHgTe, but none on complete multilayer assemblies.[2,3] Finite element modellings have been rather widely used in order to predict the appearance of stresses under thermal loadings.[4,5] However, the material properties are not well known, especially at low temperature (elastic constants, thermal expansion coefficient), and the complexity of electronic assemblies imposes many assumptions in order to obtain acceptable computing times. The different layers including single crystals are usually assumed to be isotropic and to limit the number of elements in 3D models, most authors propose to replace the interconnection layer by a homogeneously equivalent material.[6] This alternative method is efficient at decreasing the computing time and modelling the whole assembly, but only average stress values are obtained and it is impossible to show a stress gradient in each layer and to understand why the cracks initiate rather in the chip corners.

To overcome this uncertainty, x-ray diffraction (XRD) has been used to quantify the residual stresses in the different layers at room temperature after processing and after cooling at working temperature (77 K), by measuring the evolution of the lattice strain. The first works on stress analysis for single crystals by XRD were carried out by Imura in 1960; then this method was improved by Ortner by introducing a metric tensor which links measured interplanar spacings to the strain tensor.[7,8] Few studies using this method are referenced in the literature: nevertheless, it is possible to mention the work on the martensitic transformation in single-crystalline shape memory alloy or the study of stress generation in a shot-peened superalloy.[9,10]

EXPERIMENTAL PROCEDURE

The investigations have been carried out on a chip stacking corresponding to a structure used in the IR detection field. The test vehicle of this work is a 30 μm pitch 320 $\times$ 256 *I/O* pixels (15 $\times$ 10 mm^2) IR focal plane array. The architecture is presented in Fig. 1: a CdHgTe thin layer (detector circuit) is interconnected to a silicon substrate (readout circuit) by indium solder bumps with an epoxy underfill. These indium bumps are aligned parallel/perpendicular to the edges of the detection circuit, leading to an orthotropic arrangement. The crystallography of the layers is also described in Fig. 1; the CdHgTe and the silicon circuits are two single crystals (111) and (100) respectively oriented.

The complete manufacturing steps are described in some papers.[11] Four main steps can be highlighted: the indium bump deposit on the silicon circuit, the hybridisation of the CdHgTe detection circuit, the underfilling step, and to finish, the detection circuit thinning. During the hybridisation process, the assembly is subjected to a thermal load over 430 K (indium's melting temperature) which may impact the assembly reliability in a critical way. Then both mechanical and chemical polishings of the detector circuit are performed to keep the active detection CdHgTe layer very thin compared to the thickness of the silicon circuit.

Finally, this IR detector technology requires cryogenic working conditions (cold finger) to achieve maximum sensitivity. An experimental approach using the Ortner method has been considered to quantify the stresses present at room and operating temperature (77 K) in the two superimposed single-crystal layers of CdHgTe and silicon. Contrary to polycrystalline materials, the diffraction phenomenon in single crystals occurs only for particular orientations of the sample. The first step of the Ortner method is to determine the crystallographic orientation of the sample through a pole figure in order to be able to place the set up in Bragg's geometric conditions. The position of each (hkl) plane of the studied family corresponding to a combination of φ (azimuth) and ψ (tilt) angles are computed and optimised directly with the machine. Then, each (hkl) diffraction peak is acquired in a 2θ range. The inter-reticular spacings d_{hkl} are directly calculated thanks to Bragg's law:

$$\lambda = 2 \cdot d_{hkl} \cdot \sin(\theta)$$

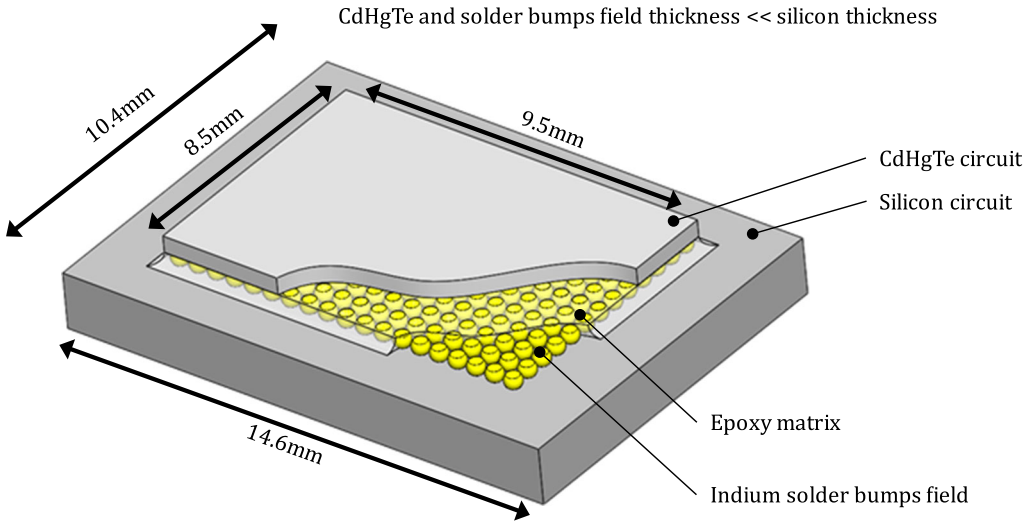
with λ as the x-ray wavelength, θ as the incident/diffracted beam angle and d_{hkl} as the interplanar spacing of the considered $\{hkl\}$ planes. At least six of their values are necessary to conduct the following calculation approach, but to obtain the most accurate values possible, it is in practice advisable to work on 12–24 multiplicity planes. The crystal strain tensor is directly determined with the strained crystal metric tensor containing the deformed lattice parameters as shown in the following expression for a cubic crystal:

$$2a^2 \cdot \varepsilon_{ij} = g_{ij} - a^2 \cdot \delta_{ij}$$

with a as the lattice parameter, ε_{ij} as the strain, g_{ij} as the strain tensor, δ_{ij} as the Krönecker symbol with $\delta_{ij} = 1$ when $i = j$ and $\delta_{ij} = 0$ when $i \neq j$.

In the reciprocal space, the metric tensor associated with the reciprocal basis is twice contravariant (noted g^{ij}). Strains are assumed to be infinitesimal and can be calculated as follows:

$$\varepsilon^{ij} = \frac{\delta_{ij} - a^2 \cdot g^{ij}}{2}$$



Layer	Crystallographic structure
CdHgTe circuit	Single crystal (111), zinc blende
Silicon circuit	Single crystal (100), diamond cubic
Indium solder bumps field	Polycrystalline, tetragonal
Epoxy matrix	Amorphous

Fig. 1. Architecture of the assembly with the crystallographic structure of each layer.

As the strain tensor is expressed in an orthonormal basis, its covariant and contravariant components are equal ($\varepsilon^{ij} = \varepsilon_{ij}$). The metric tensor components are solved with a multilinear regression of the equations given by

$$d_{hkl}^{-2} = g^{ij} \cdot a_i \cdot a_i$$

with d_{hk} as the interplanar spacing of the $\{hkl\}$ planes considered, g^{ij} as the strain tensor and a_i (i = 1–3) as the hkl node coordinates of the reciprocal lattice.

The stress values are calculated thanks to the generalised Hooke's law which links the stress tensor components to the strain tensor components ε_{kl}:

$$\sigma_{ij} = C_{ijkl} \cdot \varepsilon_{kl}$$

with C_{ijkl} as the elastic constants. To minimize the uncertainty on the undeformed material lattice parameter, a direct determination of this value is possible with the assumption

$$\sigma_{zz} = 0$$

with σ_{zz} as the stress component along the direction perpendicular to the surface of the sample. This assumption is justified by the low x-ray penetration depth (a few microns) in the material.

The experiments were performed on a four-circle diffractometer Seifert XRD 3003PTS equipped with an 1D scintillation counter detector, a post-sample monochromator and Soller slits to limit the axial divergence of the diffracted beam (Fig. 2).

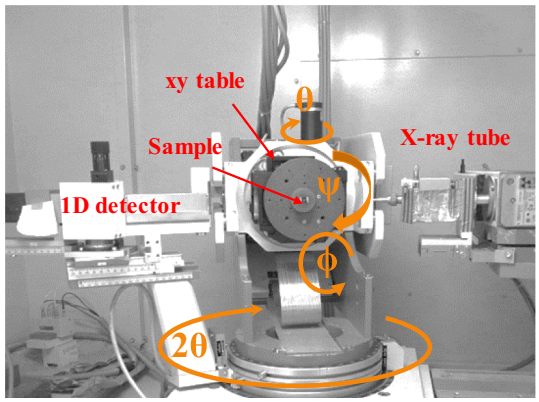


Fig. 2. Four-circle diffractometer kinematics.

The sample was placed on an xy table allowing a translation of 50 mm in the two directions to perform mappings. Two different x-ray sources were selected for the analysis of CdHgTe and silicon due to their respective lattice parameters. To obtain accurate results, two main criteria were considered:

- A diffraction angle 2θ near 150° in order to minimise the uncertainties on the strain measurements and the calculated stresses.

- Diffracted planes {*hkl*} with high multiplicity (at least 12) and a sufficient diffracted intrinsic intensity.

Moreover, to analyse the silicon readout circuit, an x-ray penetration computation was conducted: the x-rays had to pass through the CdHgTe layer and the indium solder bump field above.

According to these considerations, iron (λ = 1.9360 Å) and copper (λ = 1.5406 Å) x-ray sources were selected for CdHgTe and silicon, respectively (Table I). At room temperature, a 0.5 mm collimator was used for the CdHgTe analysis (average stress though the thickness), whereas for silicon, the loss of signal due to going through the CdHgTe and interconnection layers led to the use of a larger collimator, 1 mm in diameter, to obtain sufficient intensity and great peak definition (near-surface stress considered).

The C_{ijkl} elastic constants used for stress calculation are presented in Table II. It should be noted that no values exist in the literature for CdHgTe because it is very brittle and complicated to characterize. Due to the small difference between the elastic properties of CdTe and HgTe, authors commonly use the values of CdTe.

RESULTS AND DISCUSSION

At room temperature, several profiles were then realised considering various points in the CdHgTe chip and in the silicon circuit. For each ψ angle, the penetration depth corresponds to the entire thickness of the CdHgTe layer with the iron tube; however, it is more difficult to evaluate for the silicon circuit with the copper source due to the CdHgTe layer which attenuates the incident beam and the diffracted x-rays, but only the extreme surface is expected to be analysed (among 1–2 μm). Only the $K_{\alpha 1}$ peaks are here considered and fitted to determine the 2θ values for stress calculation, but it has been verified that the computation with the $K_{\alpha 2}$ fits gives similar results; all peaks have been fitted with a Gaussian function. Figure 3 presents three stress tensors obtained in the middle, in the corner and along the diagonal of the CdHgTe chip.

These measures show low shear stress values which can be linked to the geometric symmetries of the assembly. On the contrary, differences appear when considering σ_{xx} and σ_{yy} values: whereas the center of the chip is low stressed (almost stress-free), a compressive biaxial stress state exists in the chip corner. In order to better understand the strain/stress repartition, strain/stress XRD analyses have been carried out along several directions of the CdHgTe chip (Fig. 4b): two half diagonals and one half width of the detection circuit.

The results show a significant stress gradient, with all the chip borders analysed and under higher stress than the center; the compressive values increase gradually from the center to the border in all directions (minimum: −30 MPa). Industrially, it is often observed that the crack occurs at the chip corner after the last manufacturing step corresponding to the chemical mechanical thinning of the chip. Similar analyses have been conducted in the silicon circuit. As for the CdHgTe circuit, shear stresses are relatively low. Figure 4c presents the evolution of stress along x and y axes in the silicon. The surface of silicon in contact with the interconnection layer presents tensile stress values quite scattered from 4 MPa to 43 MPa for σ_{xx} and from 8 MPa to 41 MPa for σ_{yy}. It is to be noted that stress analyses before hybridization of the detection circuit have also been conducted in silicon at room temperature and similar values have been obtained.

To then perform XRD measurements on the IR device at low temperature, a specific cryostat has been designed (Fig. 5a) and adapted on the goniometer. The sample is fixed on a copper part cooled with an internal constant liquid nitrogen flow. A half-sphere partially transparent to x-rays placed above the sample and a vacuum circuit protect the system against ice formation. This geometry allows an optimal accessibility of the incident/diffracted beam for a great number of φ/ψ configurations. The x-ray signal loss due to the sphere is about 80%: this unfortunately excludes the possibility of analysing the silicon below the CdHgTe chip in the cryostat, which is why only the CdHgTe detection circuit has been investigated for the following experiments at low temperature. In order to obtain more signal, a 1 mm collimator diameter was used and the {620} planes were selected for the analysis (2θ = 142.6°) because of their higher diffracted intrinsic intensity. The cryostat dimensions required the *xy* table to be removed from the diffractometer which explains

Table I. XRD parameters for the analysis of both CdHgTe and silicon layers

	CdHgTe layer	Silicon layer
X-ray source	Iron	Copper
Wavelength (Å)	1.936091224	1.540601063
Crystallographic planes	{533}	{533}
Diffraction angle 2θ (°)	158.2	136.9
Collimator diameter (mm)	0.5	1

Table II. C_{ijkl} elastic constants of CdTe and silicon

	References	C_{11}	C_{12}	C_{44}	Temperature (K)
CdTe	12	53.51	36.81	19.94	298
	13	56.2	39.3	20.6	77
Silicon	14	165.64	63.94	79.51	293

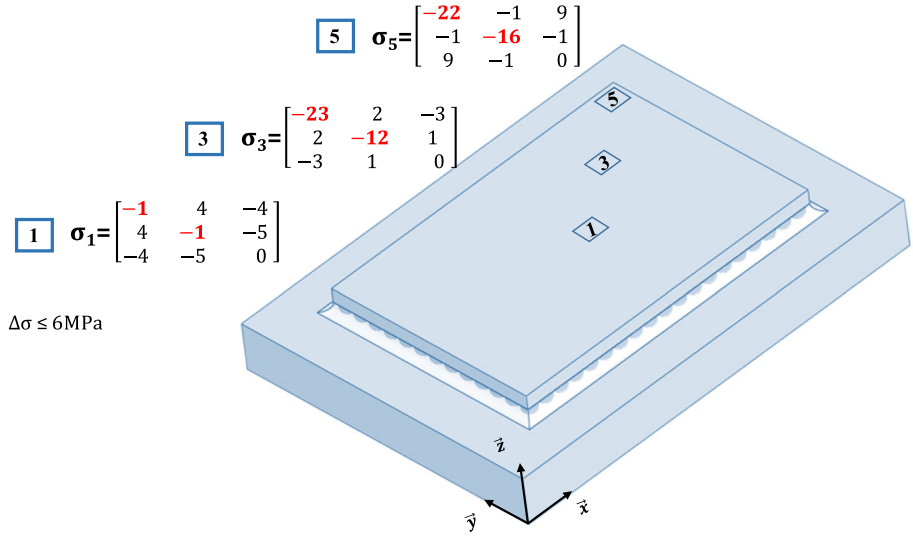


Fig. 3. Stress tensors obtained in the CdHgTe chip analysed at room temperature (all values in MPa).

why only two locations in the chip were investigated.

To be able to compare ambient and cryogenic temperature stress values, XRD analyses were carried out at the same chip locations for both temperatures (CdHgTe centre and corner). It was first showed that when using the low-temperature set up, the stress values were a little different at 293 K, especially in the centre of the CdHgTe chip (Figs. 3 and 5c). The variations could be explained by the high x-ray absorption of the half sphere made of polyethylene: it was not possible to obtain any signal for the silicon below anymore and the contribution of the extreme surface of the CdHgTe was supposed to be increased. This surface underwent both mechanical and chemical polishings which tend to induce compression stress. A significant diffraction peaks shift was then observed for the same diffracting plane (hkl) at room temperature and under cryogenic conditions (Fig. 5b): this displacement was the result of the lattice contraction and the increasing strains in the CdHgTe layer, corresponding to a lattice parameter variation of about 5×10^{-3} Å. Figure 5c presents the stress tensors obtained at room temperature and at 77 K. The evolution is similar for the two locations analysed: a biaxial tensile state occurs at low temperature in the CdHgTe circuit, with maximal stress values around 30 MPa in the corner. This thermally induced tensile stress state is due to the influence of the silicon substrate below which is thicker and retracts about twice less than the CdHgTe layer, due to the expansion mismatch of the two materials (Table III).

Today, it is known that tensile values are very unfavourable to the reliability of mechanical pieces. Previous work on InSb-based IR detectors has already shown tensile stress values induced in a thin InSb detection layer considering a similar architecture at low temperature (60 MPa at 100 K).[17] The mechanical properties of CdHgTe are not well known but the yield stress can vary from 12 MPa to 50 MPa at room temperature depending on the quantity of Zn that diffused from the CdZnTe epitaxial substrate before thinning (it has been removed during elaboration); moreover, it has very low plasticity.[18] For this material, the residual stress values measured are therefore significant; they are higher in the corners than in the centre of the chip which can be partly linked to the curvature of the detection circuit. Indeed, several numerical finite element studies on CdHgTe detector architecture report that this curvature increases at low temperature due to the difference in the

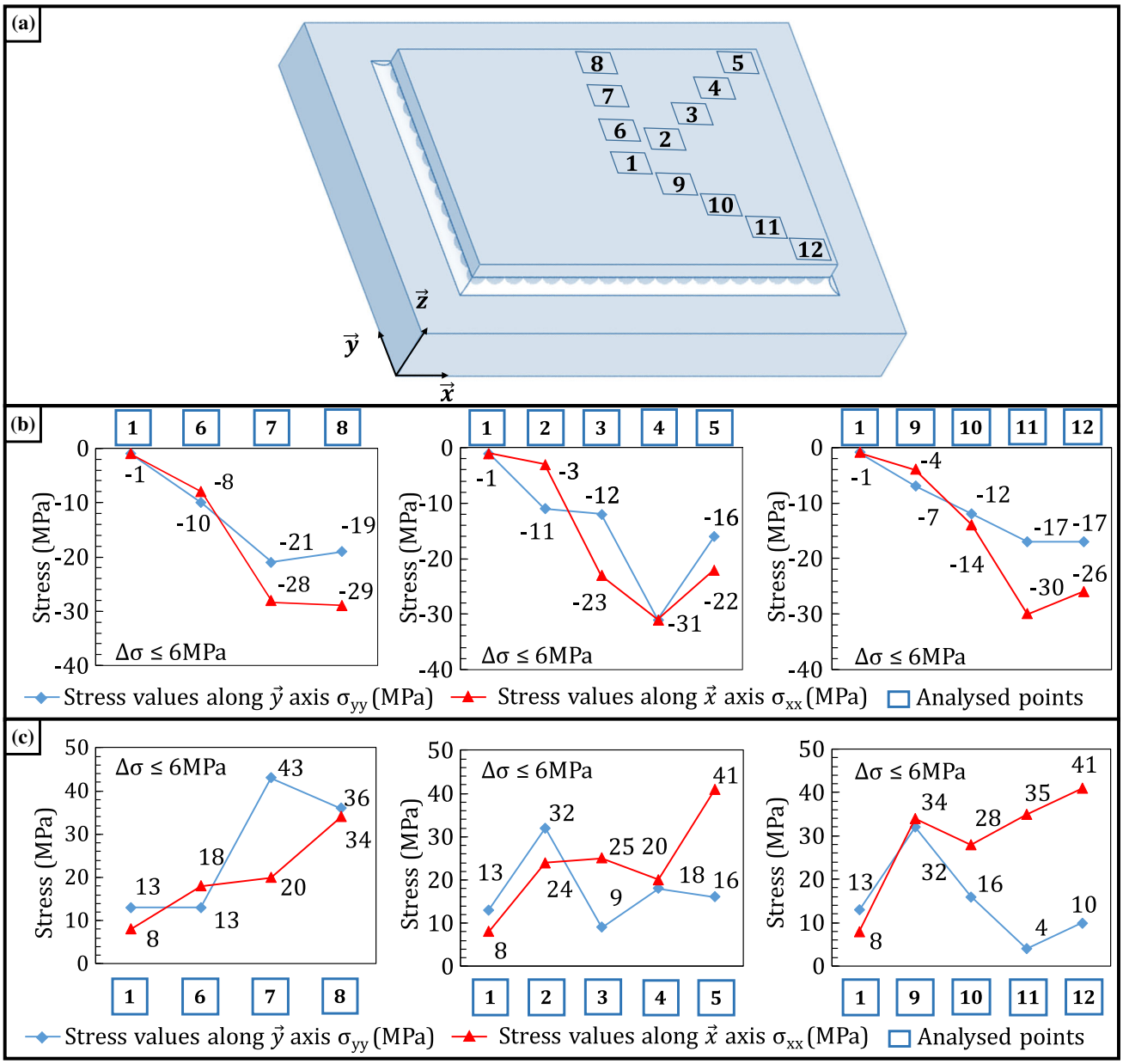


Fig. 4. (a) Analysed points in the detector (b) σ_{xx} and σ_{yy} values in the CdHgTe chip at room temperature (c) σ_{xx} and σ_{yy} values in the silicon substrate at room temperature.

coefficients of thermal expansion for the materials considered;[19] this work also reports that the Von Mises stress values are higher in the CdHgTe edges at cryogenic temperature, which is in agreement with the experimental results here presented. These high values can explain why cleavage fracture mostly occurs in these zones, as it can be experimentally observed. On the contrary, the silicon single crystal has a yield stress greater than 130 MPa, so that the measured stress values around 40 MPa are relatively low.

CONCLUSION

This work has shown that XRD is an efficient tool for stress determination at room and low temperatures in a multilayer electronic assembly. Both the thin CdHgTe detector and the silicon readout

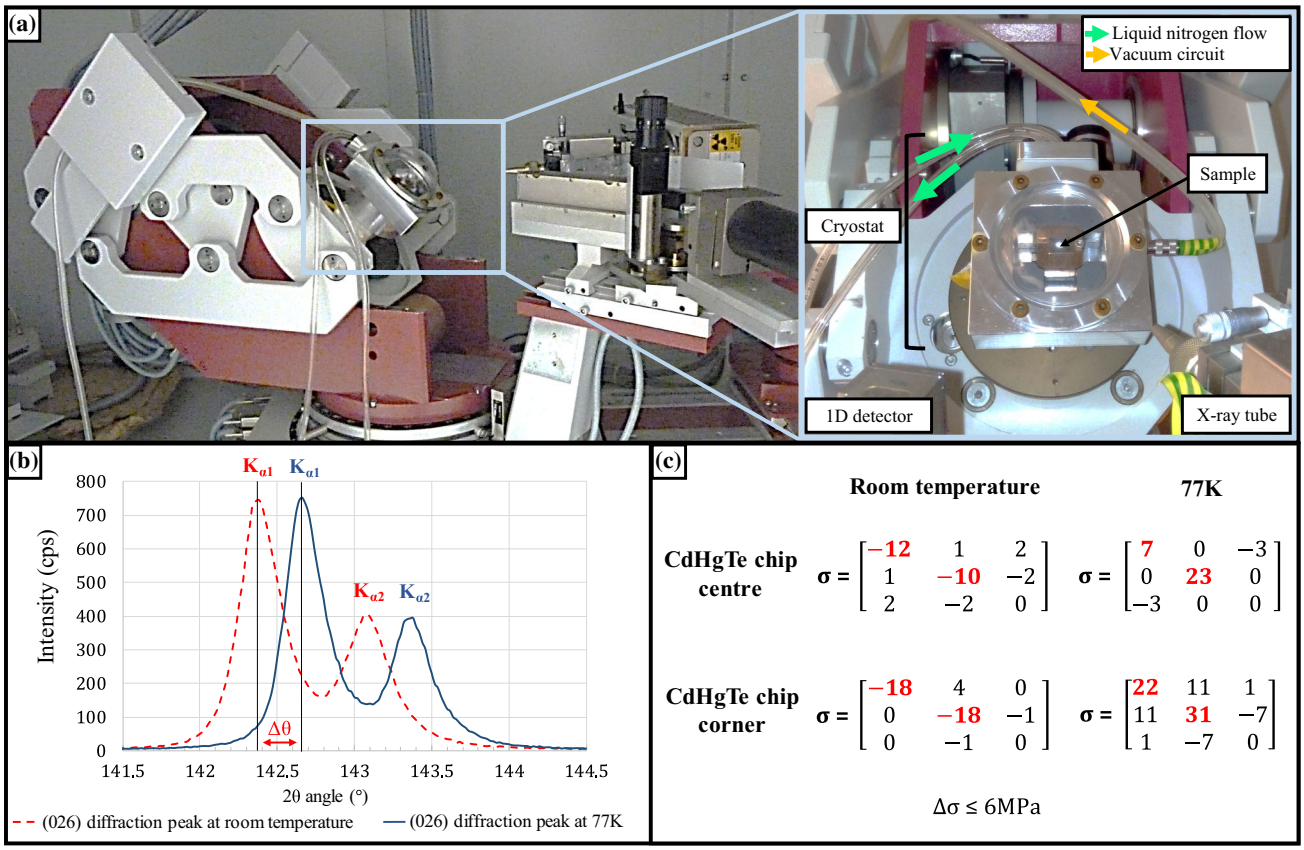


Fig. 5. (a) Experimental set up for XRD analysis at cryogenic temperature. (b) (026) Diffraction peak shift after cooling from 293 K to 77 K. (c) Stress tensors in the CdHgTe chip at room temperature and 77 K.

Table III. Expansion coefficient of the material layers

Material	Thermal expansion coefficient at room temperature (10^{-6} K^{-1})	Ratio of thermal expansion-to-substrate
Silicon	2.5[15]	1
$Cd_{0.2}Hg_{0.8}Te$	4.2[16]	1.7
$Cd_{0.7}Hg_{0.3}Te$	4.5[16]	1.8

circuits of an IR detector have been analysed. At 293 K, stresses appear to be positive in the silicon layer and negative in the CdHgTe layer, with the border close to −30 MPa. At 77 K, a tensile biaxial stress state is then observed in the CdHgTe layer, with a maximum of about 30 MPa in the corners. This value is relatively high considering the yield stress of CdHgTe and shows the direct influence of the difference in expansion coefficients of the materials used in IR detectors, which can lead to high stress values close to failure upon cooling in these zones. In order to obtain similar results with stress gradients in the CdHgTe layer using finite element methods, it would be interesting to model completely the solder bumps field and to see the influence of several parameters such as the dimensions of the chip or the crystallographic orientation of the single crystals.

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