Flip-chip technology at room temperature: A new design of microtube-based interconnect for improved mechanical and electrical properties

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A B S T R A C T

Flip-chip assembly of photonic components can be achieved at room temperature by using 10 μm pitch interconnects made of metallised oxide microtubes inserted into ductile reception pads. In order to reduce the electrical resistance of interconnects and the assembly force required, interconnect design in regard to geometry and materials used are optimised through electrical and mechanical finite elements (FEM) simulations. To reduce electrical resistance, one may increase the metallisation thickness or microtube inner diameter. To minimise the assembly force, reducing the reception pad diameter is recommended. Experiments on silicon (Si) test vehicles are conducted to validate these predictions; they indicate that there is no short circuit, with an effectiveness of 100 %. This is achieved first through the assembly of Al-0.5 $\%_w$Cu metallised oxide microtubes into Al-0.5 $\%_w$Cu reception pads, using a force less than 10 mN/interconnect and proved to have a resistance of 230 mΩ. Second, with gold (Au) metallised oxide microtubes in indium (In) pads assembled with a force less than 0.7 mN/interconnect. Last interconnects have a resistance of 670 mΩ/interconnect and can still be reduced to 500 mΩ by 2 h annealing at 100 °C.

1. Introduction

The miniaturisation and densification of microelectronic systems require continuous development, especially considering the packaging of photonic components such as infrared detectors and microdisplays, for which 3D integration is crucial. Such components consist of two parts mainly assembled using flip-chip technology: the display or detection circuit is flipped onto the top of the readout circuit in charge of the processing of the electrical signal, aligned and then bonded [1]. The aim of bonding is to achieve electrical and mechanical connection between each pixel of both circuits through an interconnect fabricated directly on the chips. This leads to use materials with very different electrical, mechanical, and thermal properties. Readout circuits are commonly Si-based, whereas the photodiodes in infrared detectors and the LEDs in microdisplays can be made of HgCdTe or InSb and GaN, respectively. The most frequently used methods for assembly include soldering, thermocompression, direct bonding [2] or even transient liquid phase diffusion bonding [3]; they entail technological hurdles to overcome in order to decrease pixel pitch down to 5 μm for advanced applications [4]. During manufacturing or in service, most of the components undergo thermomechanical loadings. Due to the difference in behaviour law and coefficient of thermal expansion (CTE) between the constitutive materials of the two chips, residual stress as well as flatness and warpage defects are induced [5] and can lead to pixel failure; interconnects must be selected so as to reduce such effects to improve reliability. The difference in CTE also results in component misalignment at high temperatures, making bonding impossible for very low pitches [6]. Last but not least, assembly solutions for microelectronics industry must be fast and easy to implement, as cheap as possible and compatible with current production tools.

In this context, assembly at room temperature appears to be a good solution with various interconnect technologies available. For example, Cu-Cu hybrid direct bonding (DBI) has started to be used, though annealing is still necessary, which increases the thermal cycle of the components [7]. Coupled with Surface Activated Bonding (SAB), hybrid technology makes it possible to achieve a very low interconnect

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resistance (80 mΩ for a 6 μm pitch) [8]. Nonetheless, this process demands a restrictive and expensive environment under ultra-high vacuum. Other technologies are based on insertion, with a contact made by plastic deformation of one or both surfaces and the formation of intermetallic compounds (IMCs) at the interface [9–15]; some consist of copper or gold bumps that are inserted into perforated reception pads [9,10]. These interconnects have a very low resistance (below 100 mΩ), but they require chemical cleaning and a high force for assembly (around 10 mN per bump), which limits the size of the components that can be bonded. Other copper interconnects with a pillar-concave structure are assembled by plastic deformation by applying a pressure of 500 MPa per interconnect at high temperature (150°C for 1 min) [11]. They show good electrical reliability, although their manufacture is currently limited to 30 μm pitch [12] and bonding requires heating. Microtubes ensuring good electrical and mechanical contact have also been developed by CEA Leti's packaging laboratory [13]. They are made of a tungsten core and are inserted in ductile reception pads. Their performance and reliability have already been demonstrated in microdisplays and infrared imagers [14]. However, their fabrication is complex and incompatible with standard foundry processes, so that current research aims at making such interconnects easy to industrialise. In general, a combined experimental/FEM approach is required to optimise interconnects design with most of the existing FEM models only considering small deformations [16–18] to deal with thermomechanical stress induced during assembly. Microtubes are subjected to high plastic deformation and need to be modelled at the pixel scale [19]. A complete insertion has still not been taken into account (about 1 μm at most) due to limited computational capabilities, which makes it challenging to optimise the microtubes design with reduced assembly force and residual stress in the different layers. Numerical models able to simulate larger deformations have recently emerged, justifying the interest in combining experiments with numerical simulations to study the assembly step [20]. As for the electrical resistance of the interconnects, it is possible to estimate them through analytical calculation. However, it is not fully representative of reality since the architecture of assemblies still becomes more and more complex, and it fails to consider the distribution of current density among the different layers. FEM models for electrical conduction analysis are more representative [21,22]; they enable to predict the global interconnect resistance and to highlight the resistive zones so as to improve the final design.

This paper proposes a new interconnect based on microtubes made of metallised silicon dioxide (SiO_2) walls inserted at room temperature into ductile reception pads. These microtubes are manufactured in very few steps, all compatible with traditional foundry processes and can be reduced down to 5 μm pixel pitch. They can reach a height of 4 μm with a wall thickness ranging from 0.3 to 1 μm, making it possible to compensate for component flatness and warpage defects. This technology operates at room temperature and is well-suited for industrialisation due to the limited use of chemicals for surface preparation (which means removal of the native oxide is not required), simplified and speed-up assembly rates, and the ability to avoid thermomechanical issues such as misalignment and generation of residual stress usually due to the difference in CTE between the readout circuit and the active chip. The objective of this work is to minimise assembly force while ensuring good electrical conductivity, through experimental and numerical investigations. It can be achieved by varying several parameters such as the interconnect geometry, the layer thickness and the materials used. The experiments conducted involve test vehicles with various designs of microtubes and reception pads, investigating their final electrical resistance. The morphology of interconnects is controlled through Scanning Electronic Microscopy (SEM) observations, with the insertion depth directly linked to the applied force during assembly. The mechanical and electrical FEM models simulate pixel-scale insertion and electrical conductivity of an interconnect for various designs. They are compared to experimental data for validation and to analyse how some parameters affect the interconnect performance.

2. Experimental procedure

2.1. Presentation of the test vehicles architecture

This study considers flip-chip test vehicles composed of a dummy detection or emission circuit (top chip) combined with a dummy readout circuit (bottom chip) through the insertion of microtubes at room temperature, as illustrated in Fig. 1. They consist of an array of around 100,000 interconnects with a 10 μm pitch (upper and lower parts are shown in Fig. 2). Both the top and bottom chips are made of Si, while the interconnects are manufactured directly onto the passivated wafer. Each pixel includes an interconnect combining an Al-0.5 $\%_w$Cu or In reception pad located on the top chip with a metallised microtube with a SiO_2 core on the bottom chip. These test vehicles have 42 identical electrical test patterns uniformly distributed across the dies. Each of them is made up of seven test circuits: two short-circuit (SC) detection patterns (testing respectively 10 and 100 interconnects) and five daisy chains (one connecting 2 interconnects, two connecting 10 interconnects and two connecting 50 interconnects), which detect open circuits (OC) and are used to determine the resistance of the interconnects. The test circuits consist of buried electrical tracks (a stacking of 10 nm titanium (Ti), 440 nm Al-0.5 $\%_w$Cu, 10 nm Ti and 40 nm titanium nitride (TiN)) connected to the interconnects by copper vias and to pads on the periphery of the bottom chip.

Three variants of interconnects have been tested, including microtubes with the same wall taper, as depicted in Fig. 2:

- Test vehicle **A1** is composed of a microtube with a low wall thickness (variant A) metallised with Al-0.5 $\%_w$Cu inserted into a reception pad of Al-0.5 $\%_w$Cu.
- Test vehicle **B1** composed of a microtube with a high wall thickness (variant B) metallised with Al-0.5 $\%_w$Cu inserted in a reception pad of Al-0.5 $\%_w$Cu.
- Test vehicle **A*2** composed of a microtube with a low wall thickness (variant A*) metallised with Au inserted into an In reception pad.

Both A1 and B1 test vehicles consist of interconnects with an Al-0.5 $\%_w$Cu/Al-0.5 $\%_w$Cu contact interface. The Al-0.5 $\%_w$Cu alloy is a low-cost material commonly used in foundries, easy to process, and has the advantage of not being subject to microstructural ageing. This should lead to facilitated diffusion mechanisms and ensure good durability. For A*2 test vehicles, Au metallisation and In reception pads have been chosen because In is a very soft and ductile material and due to their ability to form $AuIn_2$ IMCs at the Au/In contact interface to strengthen the connection. They are widely used in IR detectors [6].

2.2. Manufacture of the metallised oxide microtubes

Oxide microtubes are fabricated through a two-stage manufacturing process completely compatible with industrial foundry equipment. Firstly, the oxide core is produced via Plasma Enhanced Chemical Vapor Deposition (PECVD) with a full-plate deposit of 40 nm SiN and a 3 μm deposit of SiO_2. Photolithography then defines the shape of the microtubes (perforated discs), followed by a dry etching until the SiN layer to reveal the microtubes. The resist is removed, and the SiN is dry etched to restore contact with the Cu via at the centre of the microtubes. The next stage is linked to the metallisation process. The microtubes and vias must initially be in contact through deposits of 30 nm of Ti, 50 nm of TiN and 20 nm of Ti, done by Physical Vapor Deposition (PVD) across the entire wafer. In the case of Au metallisation, a deposit is made by PVD, leading to a thickness of 10 nm, whereas for Al-0.5 $\%_w$Cu metallisation, the PVD deposit leads to a final thickness of 100 nm for vertical walls and 150 nm for horizontal surfaces. With photolithography followed by wet etching (Au) or dry etching (Al-0.5 $\%_w$Cu), metallisation between the interconnects is finally removed to separate them electrically.

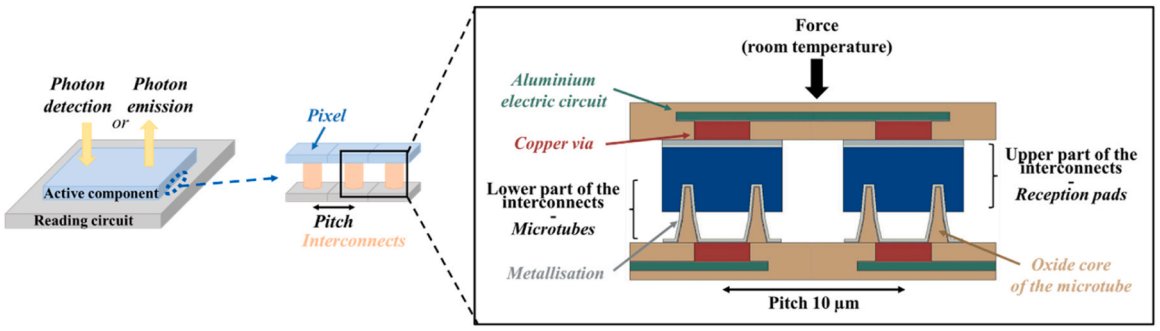
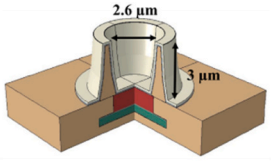
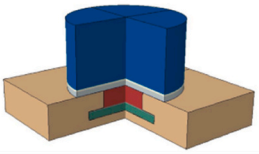
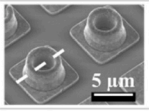
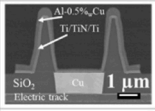
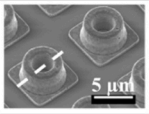
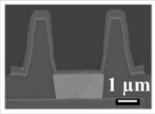
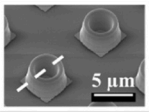
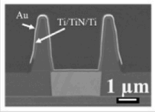


Fig. 1. Architecture of a photonic component with an interconnect composed of a microtube inserted into a reception pad at room temperature.





Lower part of the interconnects: microtube

Variant (wall thickness)	Top view SEM image	Cross section SEM image	Stacking of metallisation layers
A (300 nm)			v: 100 nm Al-0.5%$_w$Cu h: 150 nm Al-0.5%$_w$Cu 20 nm Ti 50 nm TiN 30 nm Ti
B (600 nm)			v: 100 nm Al-0.5%$_w$Cu h: 150 nm Al-0.5%$_w$Cu 20 nm Ti 50 nm TiN 30 nm Ti
*A** (300 nm)			10 nm Au 20 nm Ti 50 nm TiN 30 nm Ti

Upper part of the interconnects: reception pad

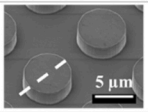
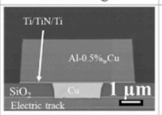
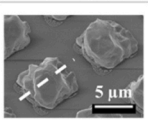
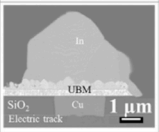
Variant (diameter)	Top view SEM image	Cross section SEM image	Stacking of reception pad's layers
1 - *Al-0.5%$_w$Cu pad* (7 µm)			2.5 µm Al-0.5%$_w$Cu 10 nm Ti 40 nm TiN 10 nm Ti
2 - *In bump* (6.5 µm)			3.5 µm In Underbump metallisation (three metallic layers with Au finish)

Fig. 2. Top view SEM images, cross section SEM images, constitutive materials and dimensions of the different microtubes and reception pads (v: vertical; h: horizontal).

2.3. Manufacture of the reception pads

Al-0.5 %$_w$Cu pads only require one single major step fully compatible with industrial equipment to be manufactured. Initially, layers consisting of 10 nm Ti, 40 nm TiN, 10 nm Ti, and 2.5 µm Al-0.5 %$_w$Cu are deposited on wafer via PVD. Photolithography is then used to define the circular patterns of the pads, followed by dry etching stopped on SiO_2 to remove excess metal and achieve electrical isolation between the pads.

The manufacturing process of In pads is composed of two major steps:

- Under bump metallisation (UBM) is deposited including three layers of metal with Au finish beneath the pads. Then, a first photolithography is performed to match the shape of the pads and an etching is carried out to electrically isolate the UBMs from each other.
- A second photolithography with resist is achieved to get cavities on the UBMs as 'mould' of In pads: they are filled by evaporated In and the excess resist is removed through a lift-off process.

It can be noticed that the evaporation process of In does not allow to obtain a perfect cylindrical shape as with the Al-0.5 %$_w$Cu PVD deposit, resulting in a rougher pad shape.

2.4. Presentation of the assembly method

The bonded test vehicles in this study are assembled using FC300 flip chip equipment from *Smart Equipment Technology* (SET), which guarantees alignment accuracy of down to 0.3 µm. The top chip featuring reception pads is flipped onto the bottom chip containing the microtubes. This process involves checking the parallelism of the two chips and aligning them through patterns on the chips. A double-headed microscope is placed between the chips for optical alignment. The top chip is then positioned close to the bottom one and, upon contact detection, a force is gradually applied until a programmed maximum force is reached. It is maintained for a given time, then progressively released. To protect the interconnects from the environment, an underfill (epoxy resin curing at room temperature) is then applied to fill the gap between the chips.

For each test vehicle, several bondings are conducted, corresponding to various maximum forces applied. The top chip is slowly raised at a speed of 40 µm/s towards the bottom chip until contact is detected. Then, a force is applied at a rate of 10 N/s, the maximum force is maintained for 1 s and the unloading is carried out at a speed of 50 N/s. The assembly force per interconnect applied is between 9.7 and 13.6 mN for B1 test vehicle, between 6.8 and 9.7 mN for A1 and between 0.2 and 0.7 mN for A*2.

2.5. Characterisation of the samples

The electrical characterisation of the test vehicles is performed using a manual prober. The measurements involve applying a current between the two tungsten tips of the prober placed on the pads (on the periphery of the bottom chip) connected to the extremities of each test circuit. A source meter connected to the system applies the current and measures the potential difference between the two tips. In a SC pattern, the two test pads are each connected to an independent electrical track and to interconnects, without the two tracks being connected to each other. Thus, if a potential difference is measured, it means that at least one SC has occurred between two interconnects, connecting the two electrical tracks together and closing the circuit. In a daisy chain, the two pads are connected to a single electrical track that connects a series of interconnects alternately from bottom to top and from top to bottom. If a potential difference can be measured, it means that there is no OC in the current path and the resistance of the chain can be determined using Ohm's law. Once measurements are done on all the daisy chains present on a test vehicle, the resistances measured are plotted as a function of the number of interconnects connected by each daisy chain (leading to high values of several tens of Ω). This enables the resistance of an interconnect (half-length of top electric track connecting two interconnects/top via/reception pad/metallised oxide microtube/bottom via/half-length of bottom electric track connecting two interconnects) on the test vehicle to be determined by the slope of the straight line passing through the plotted points. This method allows two-probe measurements to be taken to quantify the average resistance of an interconnect, without taking into account the intrinsic resistance of the system. The resistance data presented in this work correspond to the averages of the minimum measured values. To quantify OCs and SCs, we consider the percentage of test circuits that experienced an OC or SC, regardless of the number of interconnects they connect.

A *Jeol* JSM-IT500HR SEM is used to observe each interconnect's integrity, including the geometric and morphological characterisation and the determination of the microtubes' insertion depth into reception pads. The interconnect zone is accessed by cutting the samples and ion polishing using *Leica*'s TIC3X Triple Ion Beam Cutting (TIC) equipment. For samples containing In, TIC is used with a cryogenic chamber cooled to −100 °C owing to its low melting temperature of 156 °C. In order to be representative of the entire test vehicle, both directions of the bonded circuit (x and y) are considered for each sample. It should be noted that for a given assembly force, the average insertion depth of the interconnects is presented and varies by ± 150 nm from one test vehicle to another.

3. FEM models

FEM models have been generated with ABAQUS® software in order to predict the assembly force and the electrical resistance of the interconnects based on their design. Additionally, the models can forecast the stress and strain distribution in each layer and the changes in the current density through them.

3.1. FEM mechanical model

A mechanical model has been developed in this study to simulate the assembly process at pixel scale. ABAQUS/Standard is used to conduct a "static" analysis, providing detailed results down to an insertion depth greater than 1 μm. Given the interconnect geometry, the problem is 2D axisymmetric. Fig. 3 describes the geometry, mesh and boundary conditions, with a focus on the B1 test vehicle. The axisymmetry axis is represented by the yellow dotted line. The dimensions of each part are gathered from SEM observations of the microtubes and reception pads before bonding. The chips are depicted in a simplified manner: on the top side, with a SiO_2 substrate and a 2.5 μm thick Al-0.5 $\%_w$Cu reception pad, and on the bottom side, with a SiO_2 substrate and a microtube that is covered with two layers of metallisation (100 nm TiN and an Al-0.5 $\%_w$Cu layer similar to that experimentally deposited). At the interface between the metallisation and the reception pad, a "surface-to-surface" contact is established; a "hard" contact pressure-overclosure relationship is used for surface-based contact, assuming that the interaction between contacting bodies is frictionless. Considering the boundary conditions, initially, the lateral displacements (x direction) of the substrates are constrained and the bottom surface of the bottom chip is anchored (all displacements and rotations are restrained). The assembly process consists of two stages: insertion, during which a vertical displacement (y direction) of 2.5 μm is applied, and discharge, where the displacement is deactivated. The standard model is meshed using

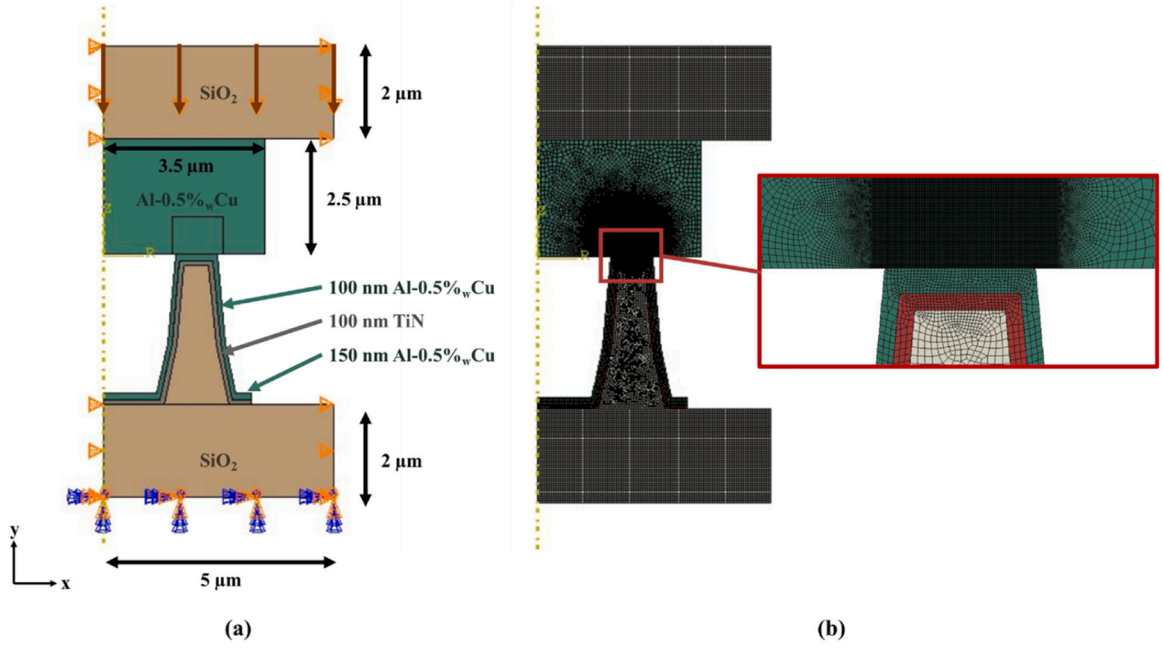


Fig. 3. 2D axisymmetric FEM mechanical model of the B1 test vehicle: (a) geometry and boundary conditions and (b) mesh.

48,291 eight-node axisymmetric elements (CAX8) including 147,069 nodes. The mesh is refined in the contact zone and a convergence analysis has been realised to provide the best possible representation of the deformation.

3.2. FEM electrical model

The electrical FEM model is generated using ABAQUS/Standard through a "coupled thermal-electrical" analysis, excluding the thermal parameters. Rather than an axisymmetric model, a 3D model incorporating all layers present in the test vehicles and electrical tracks has been developed. The model is detailed in Fig. 4. The contact between all layers is assumed to be ideal. The analysis is instantaneous (only one time increment is required), simulating a steady state. For the boundary conditions, a potential difference of 4 V is applied between two opposite surfaces of the interconnect. The model is meshed using 1,426,086 3D quadratic tetrahedrons (DC3D10E) including 2,050,942 nodes. The mesh has been refined in order to have enough elements in thin layers and has been optimised by a convergence analysis.

The electrical model calculates the current density distribution across the interconnect. The resistance R of the simulated interconnect similar to the experimental one can be determined by applying Ohm's law:

$$U = R \times i \tag{1}$$

where U represents the potential difference across the interconnect (a positive potential is applied on the top electric track end section and a negative potential is applied on the bottom electric track end section, as indicated by red arrows on Fig. 4 **(c)**) and i is the calculated current at one end of the interconnect. Actually, the resistance is determined separately for each end section of each layer of material forming the electric track (Ti/Al-0.5 $\%_w$Cu/Ti/TiN), where the potential is applied at + 2 V; the current density in each section is then multiplied by the cross-sectional area of the layer. The resistance of each layer is obtained by dividing the potential difference across the interconnect by this value. As the layers of the electric track are similar to resistors in parallel, the inverse of the interconnect resistance is equal to the sum of the inverses of the resistances of each layer section at the end of the interconnect:

$$R = \frac{1}{\sum \left(\frac{j_c \times S_c}{U} \right)} \tag{2}$$

where j_c indicates the current density at the end of a layer and S_c refers to the cross-sectional area of the layer at the end of the interconnect.

3.3. Material properties

The FEM model aims to enhance the interconnect design. To get as close as possible to reality, the electrical and mechanical properties of the materials used in the test vehicles are taken from experimental results and literature; they are summarised in Table 1 and Table 2, respectively. To get as close as possible to reality, the yield stress of both In and Al-0.5 $\%_w$Cu are determined by calibrating numerical models with experimental results. From an electrical point of view, Al-0.5 $\%_w$Cu has an intrinsic conductivity (close to that of pure aluminium) almost three times greater than In. It should be noted that the behaviour laws of the two materials used in reception pads, Al-0.5 $\%_w$Cu and In, are significantly different: In is four times less stiff than Al-0.5 $\%_w$Cu and the yield stress is twelve times lower. An elastoplastic behaviour law is defined for these two materials, whereas the others are approximated as purely elastic. In is considered with a maximum stress of 29 MPa whereas Al-0.5 $\%_w$Cu exhibits isotropic strain-hardening with a maximum stress of 460 MPa for 100 % strain.

Table 1
Electrical properties of the materials used in the test vehicles [23].

	Al-0.5 $\%_w$Cu	In	SiO_2	TiN	Ti	Cu	Au
Electrical conductivity ($\Omega^{-1}.\mu m^{-1}$)	36	12.5	10^{-14}	5	2.5	59.5	44

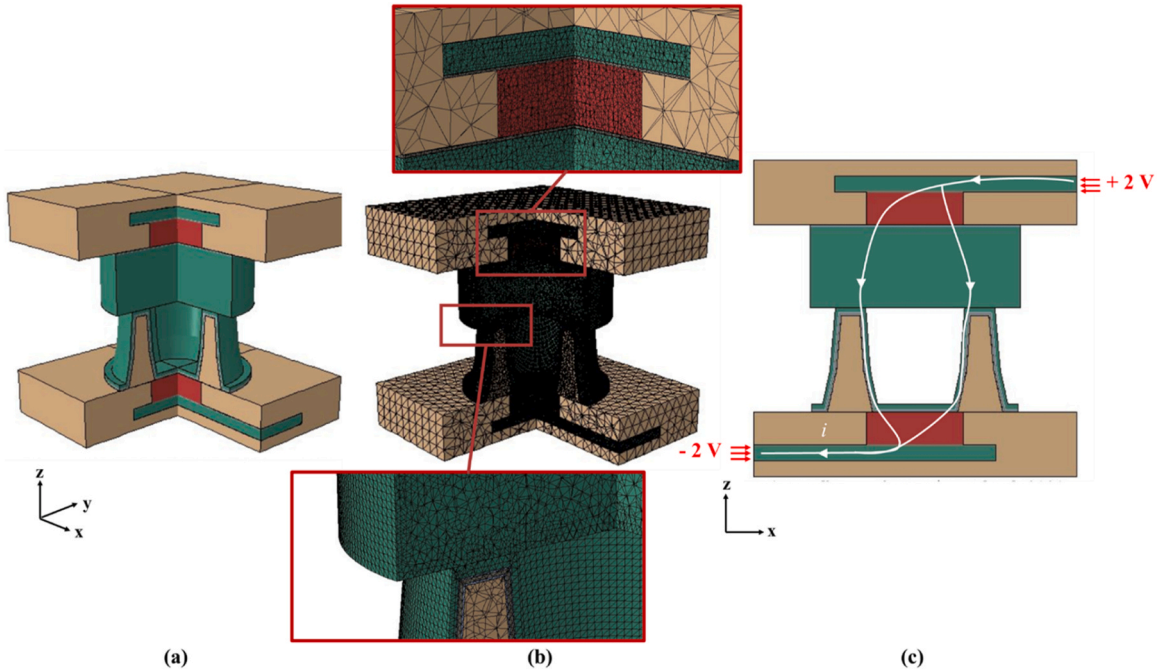


Fig. 4. 3D FEM electrical model of the B1 test vehicle: (a) geometry, (b) mesh and (c) boundary conditions.

Table 2
Mechanical properties of the materials used in the test vehicles.

	Al-0.5 $\%_w$Cu	In	SiO_2	Au	TiN
Young's modulus (GPa)	52 [24–27]	13 [28]	65 [29–32]	90 [33]	500 [34]
Poisson's ratio	0.35 [24,25,27]	0.45 [28]	0.25 [29]	0.45 [33]	0.25 [34]
Yield stress (MPa)	110 [35–37]	8.93 [38]	364 [30–32,39]	300 [40–42]	> 1000 [43]

4. Results

4.1. Macroscopic characterisation of B1 test vehicle

Several assembly forces have been applied to the B1 test vehicle to verify the accuracy of FEM models. Fig. 6 shows the evolution as a function of the insertion depth and compare it to numerical simulations. The model-derived curve shows two trends: the force increases rapidly up to a depth of 200 nm, then the slope bends and the force increases more linearly up to a depth of 1.7 µm. The simulated values are very close to the experimental forces required to create the interconnects: for example, for an insertion depth of 1.1 µm, the force is 11.6 mN for experiments while it is 11.8 mN for simulations (less than 2 % difference).

Regarding the electrical resistance of interconnects in Fig. 5, the values decrease as the insertion depth increases for both experiments and numerical simulations. However, there is a great difference for depths until 1 µm, while for the deepest insertion, they are clearly similar. For an insertion depth of 1.4 µm, it is worth mentioning that the experimental test vehicles exhibit a 100 % yield rate, with no instances of short circuits and a minimum resistance measured of 190 mΩ.

4.2. Microscopic characterization of B1 test vehicle

SEM observations have been conducted on the B1 test vehicles: Fig. 7 **(a)** displays a component assembled using a force of 11.6 mN/interconnect and the deformation of the reception pad can be compared with the mechanical simulation for the same insertion depth in Fig. 7 **(b)** and **(c)**. The distribution of the plastic deformation throughout the assembly indicates that the plastic strain is initiated at the inner and outer edges of the contact zone between the metallisation and pad, after a relative chip movement of a few nanometers. Then, the plastic zone of the pad grows almost hemispherically, spreading deeper into the pad (in y direction) and to the sides (in x direction). From 200 nm of insertion, most of the pad except the central zone has plasticised and plastic deformation still increases progressively with the insertion depth of the microtube and the contact surface between the metallisation and the pad. The FEM model (Fig. 7 **(c)**) also indicates that the metallisation undergoes compression and is stretched along the sides of the microtube during insertion, which is confirmed through SEM observations (Fig. 7 **(a)**).

SEM observations also show that the contact between the two parts of the interconnect only takes place at the top and on the inner wall (though not on the few upper nanometres) of the microtube. This is consistent with the deformed shape extracted from the FEM model, Fig. 7 **(c)**. Indeed, part of the pad above the microtube is pushed sideways during insertion, so that no contact can be established between the outer wall of the microtube and the pad. This has no influence on the final electrical conductivity as the electrical FEM model, depicted in Fig. 7 **(d)**, indicates that the current only passes through the metallisation on the inner wall of the microtube. Nevertheless, for the weakest forces applied, it is also experimentally observed that the contact interface sometimes exhibits decohesion and infiltration of underfill, which can unfortunately lead to the loss of electrical contact with the presence of open circuits.

4.3. Influence of the oxide microtube design (A1)

Test vehicle A1, illustrated in Fig. 8 **(a)**, features an oxide microtube with a wall thickness 300 nm smaller than B1. The evolution of both the assembly force and the electrical resistance as a function of the insertion depth is presented in Fig. 6 and Fig. 5, respectively, and can be compared to test vehicle B1 in order to get the impact of the design of the oxide microtube. The numerical simulations indicate that decreasing the wall thickness reduces the assembly force to below 10 mN/interconnect for insertion depths up to 1.5 µm, but it has no effect from an electrical standpoint.

The mechanical behaviour was qualitatively validated, as experimental values are close to those simulated. It is worth mentioning that when an insertion depth of 1.6 µm is reached, the test vehicles exhibit a 100 % yield rate in the measured interconnects, with no instances of short circuits and a minimum resistance measured of 230 mΩ, slightly higher than simulated values. Furthermore, the minimum resistance achieved with both the A1 and B1 test vehicles are in the same order of magnitude.

4.4. Influence of the constitutive material of the reception pad (A*2)

Test vehicle A*2, illustrated in Fig. 8 **(b)**, features an In reception pad instead of the Al-0.5 $\%_w$Cu pad for A1. It is possible to investigate the

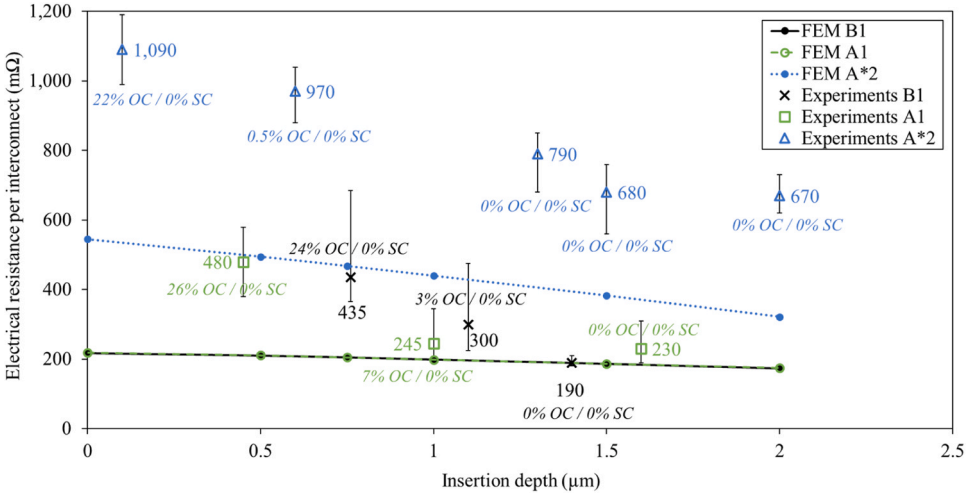


Fig. 5. FEM and experimental evolution of the electrical resistance as a function of insertion depth for the three test vehicles (with OC and SC experimental rates; insertion depth measurement uncertainty: ± 150 nm).

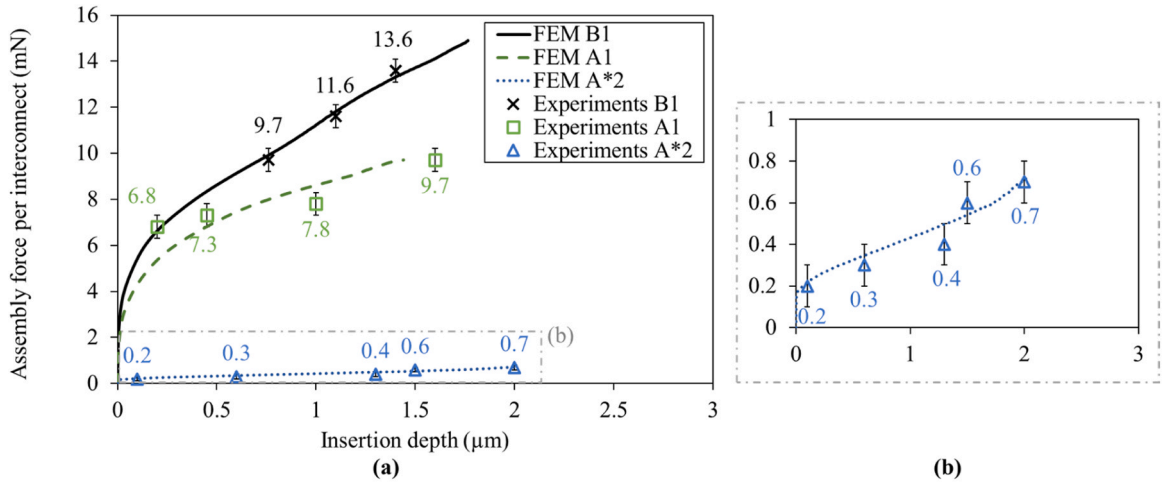


Fig. 6. FEM and experimental evolution of the assembly force as a function of insertion depth for (a) the three test vehicles with (b) a zoom for the A*2 test vehicle (insertion depth measurement uncertainty: ± 150 nm).

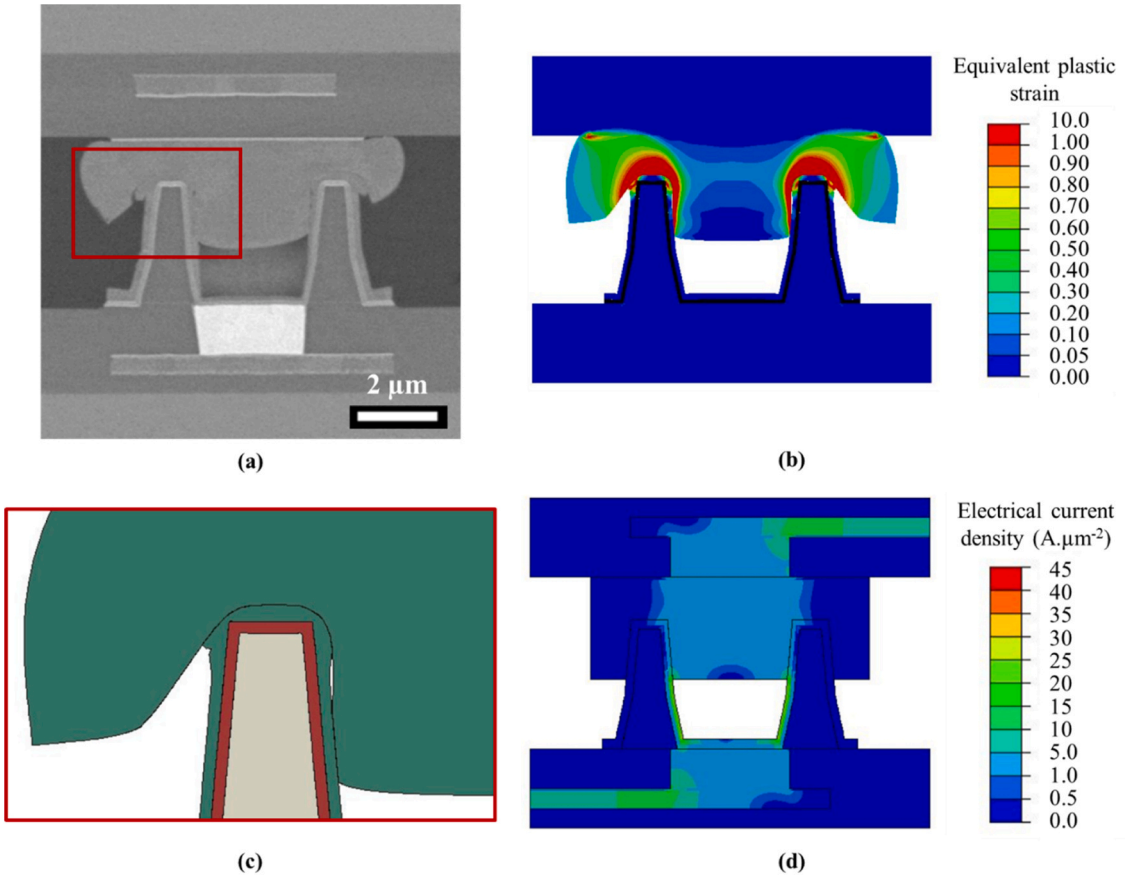


Fig. 7. Test vehicle B1: (a) SEM observation of a cross-section of an interconnect assembled using a force of 11.6 mN/interconnect, (b) distribution of the equivalent plastic deformation in the interconnect simulated with the FEM mechanical model, (c) simulated deformed shape of the interface between the metallised oxide microtube and reception pad and (d) simulated distribution of the current density through the interconnect.

influence of the material constituting the pad by comparing the evolution of the assembly force and the electrical resistance presented in Fig. 6 and Fig. 5, respectively, to previous test vehicle (A1). Numerical simulations show that substituting Al-0.5 $\%_w$Cu for In considerably reduces the assembly force required to insert an oxide microtube to below 1 mN/interconnect for insertion depths up to 2 µm. From an electrical point of view, the simulations indicate higher electrical resistance for A*2 test vehicle than for A1 and B1, due to the thickness of the metallisation.

The model predictions concerning the assembly force are confirmed by the experimental results although the predicted values of interconnects electrical resistance are significantly far from the experimental ones, even for high insertion depths: A*2 test vehicle exhibits a minimum resistance of 670 mΩ. Furthermore, an interconnect yield close to 100 % is obtained from an insertion depth of 0.6 µm and the formation of $AuIn_2$ (atomic composition determined using energy dispersive X-ray spectroscopy in SEM) IMCs is observed at room

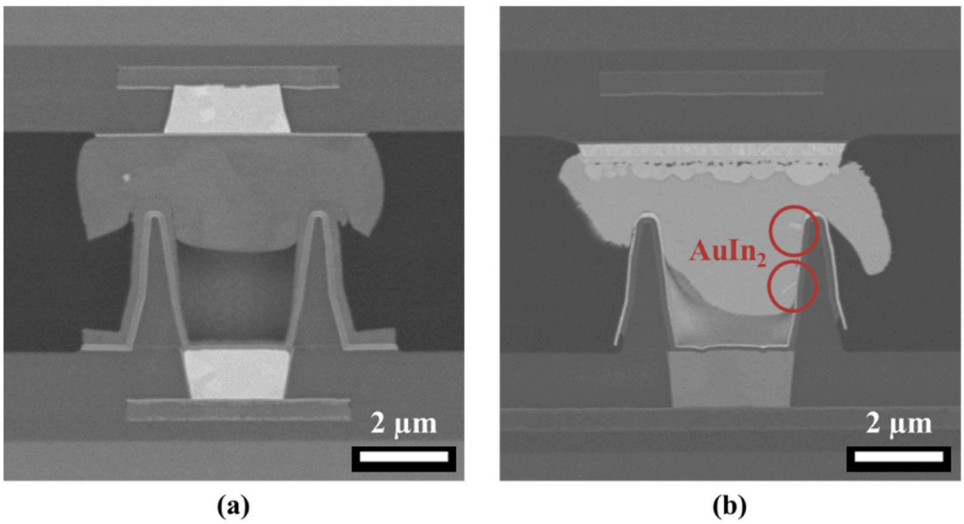


Fig. 8. SEM observation of an interconnect: (a) A1 bonded using a force of 7.8 mN/interconnect and (b) A*2 bonded using a force of 0.7 mN/interconnect.

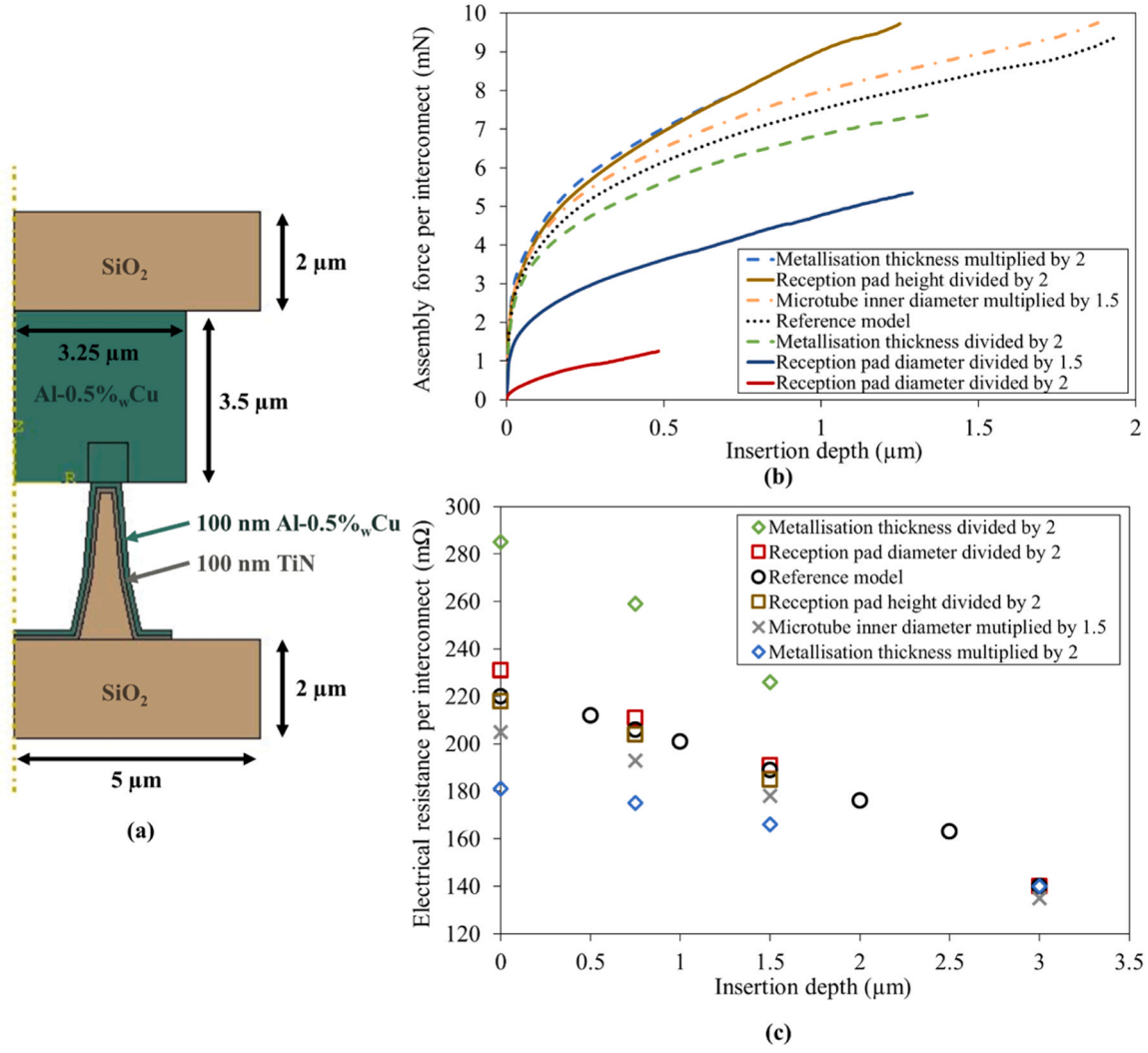


Fig. 9. FEM study of the influence of the metallisation thickness, reception pad diameter and microtube inner diameter: (a) reference model design, (b) evolution of the assembly force of an interconnect as a function of the insertion depth, (c) evolution of the electrical resistance of an interconnect as a function of the insertion depth.

temperature at the interface between In and Au (Fig. 8 **(b)**), which ensures a chemical contact between the two layers.

4.5. Influence of other parameters through numerical simulations

The same models were then used to determine the influence of other design parameters that can be manufactured without requiring extensive process development: the dimensions of the reception pad, the inner diameter of the microtube and the thickness of the metallisation. The effect of these parameters on the evolution of both the assembly force and the electrical resistance as a function of the insertion depth are shown in Fig. 9 **(b)** and **(c),** respectively, considering the reference model design in Fig. 9 **(a)**. It is obvious that some parameters such as the height of the reception pad have a low influence on the electrical resistance, although others can significantly affect the final properties:

- decreasing the diameter of the reception pad considerably reduces the assembly force from around 6.1 mN/interconnect down to 1.3 mN/interconnect for a diameter divided by 2. Additionally, it has a negligible impact on electrical resistance;
- increasing the inner diameter of the oxide microtube reduces electrical resistance (up to 15 mΩ for an inner diameter multiplied by 1.5), but this also results in an increase in the assembly force;
- increasing the thickness of the metallisation on the inner wall of the microtube significantly reduces electrical resistance if the insertion is incomplete (up to 39 mΩ for a doubled metallisation thickness). It leads, however, to an increase in the assembly force as well.

Table 3 and Table 4 summarise all the numerical results of this work.

5. Discussion

5.1. Mechanical model validation at macroscopic and microscopic scales

The characterisation of the B1 test vehicle allows to validate the predictions of the mechanical model at both macroscopic and microscopic scales. The experimental results and FEM simulations are very close whether it be for the deformations undergone by the pad and the metallisation or the assembly force values. The evolution of the force, presented in Fig. 6, can be explained by the predicted plastic strain distribution shown in Fig. 7 **(b)**. First, a great force is required to induce plasticity in the pad; then, once most of the pad has plasticized (around 200 nm insertion depth), the slope of the curve bends and the force required to insert deeper increases linearly with insertion depth and Al-0.5 $\%_w$Cu hardening. The final shape of the deformed pad depends on the morphology of the interconnect and is also well predicted by the model, as shown in Fig. 7 **(a)** and **(c)**, ensuring contact only with the inner side of the microtube.

5.2. Parameters reducing the assembly force

Some geometric parameters have a strong influence on the force necessary for assembly. The experimental results for the A1 test vehicle (Fig. 6) show that dividing by 2 the thickness of the oxide microtube wall enables to reduce the assembly force by 30 % for 1.5 μm insertion depth, down to 10 mN/interconnect, as predicted by numerical simulations. It is linked to the division by around 1.5 (between variants A and B) in the contact surface area between the pad and the top of the metallised oxide microtube. Limiting the diameter, i.e. the volume of the pad that needs to be deformed for insertion, has a similar effect (Fig. 9 **(a)),** with the force decreased by 80 % for a diameter divided by 2.

Changing the material of the reception pad from Al-0.5 $\%_w$Cu to In in A*2 test vehicle also allows to greatly reduce the assembly force (Fig. 6): the effect is huge since said force is divided by 20, down to 1 mN/interconnect, due to the low yield stress of In in comparison with Al-0.5 $\%_w$Cu.

In all cases, this provides significant benefits for the assembly of large format components (including more than 5,000,000 pixels).

5.3. Electrical model validation and limits

B1 test vehicle characterisation (Fig. 5) allowed to validate the predictions of the electrical model only for large insertion depths. The model only considers geometric resistive phenomena and ideal contact (continuous contact on all sides) whereas other parameters experimentally observed yet difficult to simulate may also play a role. For example, the irregular interface between metallisation and pad due to the native oxide layers on Al-0,5 $\%_w$Cu can provide additive resistive phenomena that increase the global resistance of the interconnect. This is particularly true at shallow insertion depth, for which contact areas are reduced as the resistive oxide layer is not broken over the entire contact surface. It generates higher interconnect resistance (here up to 435 mΩ) and many open circuits (here 24 %). When insertion depth increases, contact areas grow due to the plastic deformation of the pad, reducing the electrical resistance, which therefore tends towards the simulated value (for an insertion depth of 1.4 μm). In addition, the lack of contact between the deformed pad and the metallisation on the outer wall of the microtube, due to the structure of the interconnect, does not limit electrical conduction; indeed, FEM current density distribution in Fig. 7 **(d)** shows that the current only flows through the metallisation on the inner wall of the microtube. Overall, the final electrical resistance value measured for this type of interconnect fulfills the requirements because it is lower than 1 Ω. Nevertheless, to ensure optimal interconnect performance (no open and short circuits), it is necessary to attain a

Table 3
Summary of FEM results for test vehicles (B1, A1 and A*2) compared to B1.

Design parameters	Assembly force (1 μm insertion depth)	Electrical resistance (1 μm insertion depth)	Comments
B1	11 mN	200 mΩ	Greater experimental values at shallow insertion depth
A1 Microtube wall thickness divided by 2	- 23 %	=	Greater experimental values at shallow insertion depth
A*2 Change in pad/metallisation material	- 95 %	+ 120 %	Thinner metallisation Greater experimental values

Table 4
Summary of FEM study results of the influence of other design parameters compared to the reference model.

Design parameters	Assembly force (1 μm insertion depth or 0.5 μm*)	Electrical resistance (1 μm insertion depth)
Metallisation thickness divided by 2	- 9 %	- 25 %
Metallisation thickness multiplied by 2	+ 15 %*	- 15 %
Reception pad diameter divided by 2	- 80 %*	- 2 %
Reception pad height divided by 2	+ 20 %	- 1 %
Microtube inner diameter multiplied by 1.5	+ 6 %	- 6 %

sufficient insertion depth.

5.4. Improvement of the electrical conductivity

Decreasing the thickness of the oxide microtube wall has no impact on electrical performances as presented in Fig. 5. A1 and B1 test vehicles exhibit the same electrical resistance tending towards simulated values at high insertion depths, because the inner diameter of the microtube does not change and the current flows only through the inner part.

Modifying the material of the reception pad from Al-0.5 $\%_w$Cu to In has no significant impact on the electrical resistance either. Even though In is less conductive than Al-0.5 $\%_w$Cu for the pad, Au is more conductive than Al-0.5 $\%_w$Cu for the metallisation, which compensates considering the whole interconnect. Nevertheless, A*2 test vehicle has a thinner Au metallisation compared to the Al-0.5 $\%_w$Cu metallisation of A1 test vehicle, leading to simulated values multiplied by around two (Fig. 5). The measured electrical resistance of this interconnect deviates from simulated values due to the non-continuous contact observed between the pad and the metallisation. Indeed, if the contact had been ideal, $AuIn_2$ IMCs would have been created everywhere along the inner wall and the Au layer would have been entirely consumed, but only some IMCs grains are observed in Fig. 8 **(b)**. The native oxide layer on In pad probably acts as resistive barrier at the interface, explaining the high values of resistance. This way, only small contact points are created between the metallisation and the In pad, restricting the flow of current and adding resistive phenomena to the interconnect. However, the measured values remain reasonable since less than 1 Ω, and a 100 % yield without short-circuit is achieved from very shallow insertion depths, probably due to the formation of IMCs which form a connection between the microtube and the pad as soon as they come into contact. The electrical resistance of In-based interconnect can still be minimized, down to 500 mΩ, even for initial values close to 900 mΩ, by annealing for 2 h at 100 °C after assembly, as illustrated in Fig. 10. This heat treatment leads to the diffusion of Au in In and the growth of $AuIn_2$ IMCs at the interface for a better contact, all the more so as the electrical conductivity of such IMCs is 18 $\Omega^{-1}.\mu m^{-1}$ [44], i.e. significantly higher than that of In.

Finally, FEM simulations also show in Fig. 9 **(c)** that modifying the design of the interconnect can greatly reduce the electrical resistance: first by increasing the inner diameter of the microtube to create a larger contact surface between the reception pad and the inner wall of metallisation, then by increasing the metallisation thickness to enlarge the cross-sectional area through which the current flows.

6. Conclusion

This paper investigates new 10 µm pitch interconnects based on metallised oxide microtubes inserted in ductile reception pads for the assembly of photonic components. The aim was to optimise the design in order to reduce assembly force and minimise the electrical resistance of the interconnects. Mechanical and electrical FEM models were used to predict the influence of several parameters and the results were compared to experimental measurements on test vehicles at both macroscopic and microscopic scales.

The results showed that increasing the wall thickness of oxide microtubes increases the bonding force without affecting the electrical resistance. They also pointed out the advantages of selecting In as material for the reception pad, which may decrease the bonding force (by a factor of 20 for the same insertion depth) despite its unfavourable impact on electrical resistance. Nevertheless, this can be improved by gentle annealing (2 h at 100 °C) leading to the formation of $AuIn_2$ IMCs for a final electrical resistance around 500 mΩ.

A 100 % interconnect yield can be achieved without short circuit occurrence by inserting variant A metallised oxide microtubes into:

- Al-0.5 %wCu pads with a force per interconnect of 9.7 mN leading to a resistance per interconnect of 230 mΩ;
- In pads with a force per interconnect of 0.7 mN leading to a resistance per interconnect of 670 mΩ.

Finally, the models highlight the geometric parameters to optimise in order to enhance the performance of interconnects. For instance, minimizing electrical resistance can be achieved by increasing the thickness of the metallization or raising the inner diameter of microtubes, and decreasing the diameter of reception pads can reduce the assembly force.

Future work will investigate the reliability of this new interconnect (thermal shocks, ageing) and quantify its adhesion by measuring bonding strength using shear/pull tests.

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CRediT authorship contribution statement

Natacha Raphoz: Writing – review & editing, Validation, Supervision, Resources, Project administration, Funding acquisition. **Boris Piotrowski:** Writing – review & editing, Validation, Supervision, Software, Resources, Methodology, Investigation, Conceptualization.

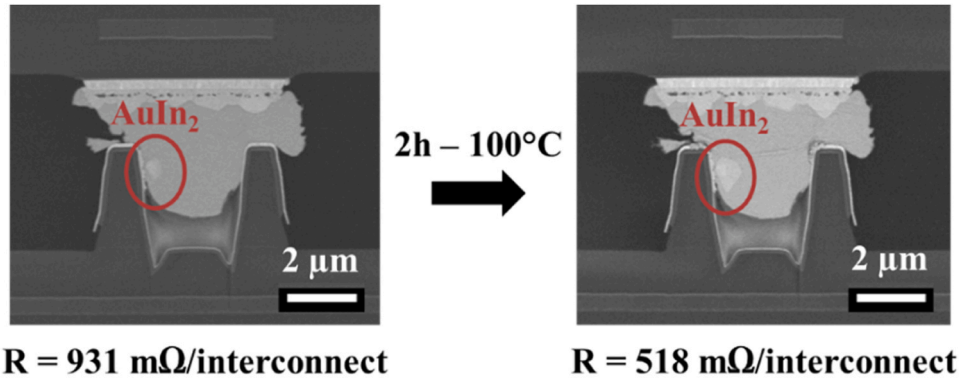

Fig. 10. Reduction of the electrical resistance and growth of IMCs $AuIn_2$ before and after 2 h annealing at 100 °C.

Olivier Mailliart: Writing – review & editing, Validation, Supervision, Resources, Project administration, Funding acquisition, Conceptualization. **Cloé Desbordes:** Writing – review & editing, Writing – original draft, Visualization, Validation, Software, Resources, Project administration, Methodology, Investigation, Formal analysis, Conceptualization. **Raphaël Pesci:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

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