Reduce Order Modeling of the modular multilevel DC/DC converter (M2DC) for HVDC grid

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***Index Terms*—M2DC, Modelling, Modular Multilevel Converter (MMC), DC-DC converter, Power system stability, Multi-terminal HVDC, Reduce Order Model.**

***Abstract*—The Modular Multi-Level DC-DC Converter (M2DC) is an attractive non-isolated DC-DC converter topology for HVDC grid. In order to carry out MTDC grid stability studies, the development of reduce order models of converters is necessary. This article first presents the M2DC converter. Then, the reduce order model will be developed in the second part. The development of the control of this model will be carried out in the third part. Atlast, the comparison of the reduce order model and its control with the average arm model will be performed in the later section of the paper.**

The upper and lower arm are precised with the subscript "u" and "l".

P^*	Reference power on low-voltage side
C_{SMu};C_{SMl}	Capacity of sub-modules
C_{totu};C_{totl}	Equivalent capacity of arm
i_s	Current on low-voltage side
i_{diff}	Differential current
v_{diff}, v_s	Decoupled modulated voltages.
v_{Ctotu};v_{Ctotl}	Voltage of equivalent capacity of arm
N_u,N_l	Number of sub-module in the half-arm
n_u,n_l	Number of active sub-module in the half-arm
v_{mu};v_{ml}	Modulated voltages
φ	Angle between the AC component of v_{ml} and $-v_{mu}$
T,ω	Period and pulsation of AC variables
θ	Angle between i_{sAC} and i_{diffAC}
θ_v	Angle between v_{sAC} and v_{diffAC}
r, l	Arm resistance and inductance
r_s, l_s	Line resistance and inductance
W_c^{Σ}	Energy stored in the arm
W_c^{Δ}	Difference of energy stored between the upper arm and the lower arm.

I. INTRODUCTION

Over the past two decades, many HVDC links have been commissioned and many more will be in the near future. Multi-Terminal DC (MTDC) grids have been proposed interconnecting these HVDC point-to-point links to increase their flexibility and robustness. However, existing HVDC system interconnections will require bi-directional DC-DC converters since voltage levels and grounding systems may vary between projects. However, the voltage levels in HVDC prohibit the use of conventional topologies, switching type. As presented in [1] to [5], major topologies for DC/DC converters in the high-voltage area are based on the Modular Multilevel Converter (MMC) architecture, thanks to its modular property, high efficiency and growing technological maturity. Among these different proposals, the MMC Dual Active Bridge (MMC DAB) [5] [7] and also the Modular Multi-level DC-DC converter (M2DC) [5] [6] are attractive. The first one is an isolated DC/DC converter since it is composed by two MMC converters

connected to each other on AC side with a medium frequency transformer [7]. The second one, the M2DC converter, is a non-insulated DC/DC one and is less studied. Its schematic is presented in Fig.1 [6].

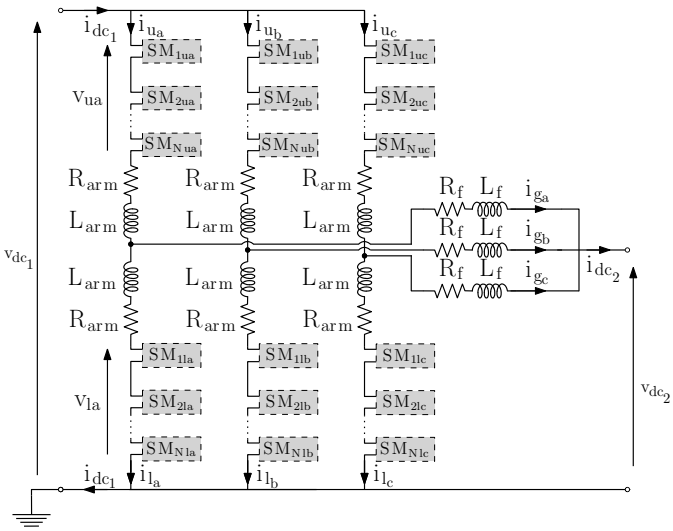

Fig. 1. Modular Multilevel Converter (M2DC) Schematic.

Control problems have been identified in the MMC literature, as reported in [8]. During the last decade, the design, modeling, and control of the original AC-DC version of the MMC have been largely studied but for the M2DC, these elements have been less focused [7] [9] [10].

MTDC grid stability studies, based on models of reduced phasor-model for MMC converters [11], have been carried out in recent years [12] [13]. However, the study of these MTDC grid remains a challenge if the latter incorporates a DC/DC converter. Indeed no reduced model of DC/DC converter for HVDC is available except if the DC/DC topology is based on the MMC topology in AC/DC version like the MMC DAB.

This paper, in the first part presents the M2DC principles. In the second part, the Kirchhoff's laws will be used to establish a Reduce Order Model (ROM). This part will be splitted in three sections to develop the ROM model connected to each DC side and the third section will link both side to the global energy stored into the M2DC. The development of the control of this model follows in next part. Validation of both the model and its control will be carried out at a later stage.

II. Average arm model and static analysis of the modular multilevel DC converter (M2DC)

The Modular Multilevel DC Converter (M2DC), described in fig. 1, is composed of at least two interleaved legs, interconnected across the two DC terminal voltages. Each leg consists of two arms made of series-connected Sub-Modules (SMs). The topology of these SMs can be either of half-bridge and/or full-bridge types depending on the case, if a DC-fault blocking capability is required on one DC bus or another, since it could require a negative voltage capability. Therefore, the number of SMs and its technology can be different for the upper arm compared to the lower one.

The M2DC offers an attractive insulated topology since it inherits some advantages from MMC, namely low switching frequency of individual semiconductors and low harmonic content in the current waveform. Furthermore, the M2DC requires fewer sub-modules (SM) compared to the "Dual Active Bridge MMC topology" since the stacks only process a part of the total converter power. This limits its overall cost and power losses (when a similar balancing control algorithm and therefore a similar switching frequency are used).

The analysis of the topology and the design of the control are focused on a single leg to simplify the presentation and will be generalised after that. Due to the large number of SMs in the M2DC, a simplified averaged arm model, fig. 2, is used for dynamic and steady-state analysis. This simplified averaged arm model is agnostic to the types of SMs used (e.g. half or full bridges) and considers that the balancing control algorithm of the voltage of each sub-module is operating properly.

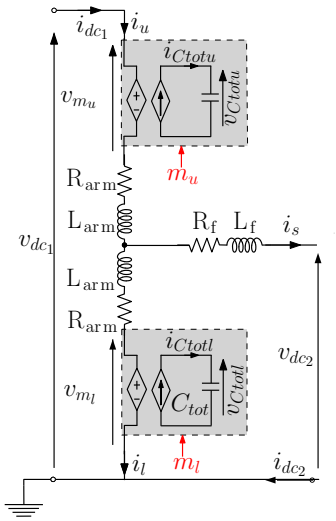

Fig. 2. Equivalent average M2DC arm model.

For each arm, it is possible to define a modulated voltage v_{mj} and a modulated current i_{Ctotj} where j represents the upper (u) or the lower (l) arm:

$$\begin{cases} v_{mj} = m_j.\, v_{Ctotj} \\ i_{Ctotj} = m_j.i_j \end{cases} \quad \text{with} \quad m_j = \frac{n_j}{N_j} \tag{1}$$

$$C_{tot}\frac{dv_{Ctotj}}{dt} = m_j.i_j \quad \text{with} \quad C_{tot} = \frac{C_j}{N_j}. \tag{2}$$

v_{Ctotj} is defined as the sum of all the SMs capacitor voltages in the j arm. 1 and 2 are identical to an ideal chopper connected to an equivalent capacitor could therefore replace all arm SMs. This equivalent average model of a M2DC leg is presented in the gray box of fig. 2.

Consider v_{mjDC}, the DC components of the modulated voltage of j arm and i_{jDC}, the DC components of the arm j current. If the resistances and the submodules losses are neglected, v_{muDC}, v_{mlDC}, i_{uDC}, i_{lDC} can be expressed as in (3).

$$\begin{aligned} v_{muDC} &= v_{dc_1} - v_{dc_2} \qquad & i_{uDC} &= i_{dc_1} \\ v_{mlDC} &= v_{dc_2} & i_{lDC} &= i_{uDC} - i_{sDC} \end{aligned} \tag{3}$$

Consider P, the power flowing through the arm from one DC side to the other, then the DC powers of the upper and lower arms is given in (4).

$$\begin{aligned} P_{uDC} &= v_{muDC}.i_{uDC} = (1-\alpha).P \\ P_{lDC} &= v_{mlDC}.i_{uDC} = (\alpha-1).P \end{aligned} \text{with } \alpha = \frac{v_{dc2}}{v_{dc1}} \tag{4}$$

As showed by the above equation the DC power flowing in the arm is opposite in each arm but more importantly it is non-zero. So, the energy stored in the capacitors will diverge. To avoid this, AC components are needed in the converter in order to nullify the average power of the arms. To avoid AC current into DC sides, the M2DC internal AC currents must have the same amplitude and a phase shift equal to 2π/m for a M2DC with m legs.

The Kirchhoff's laws applied on the M2DC gives the following equations :

$$i_s = i_u - i_l \tag{5}$$

$$\begin{aligned} v_{dc1} = L_{arm}(\frac{di_u}{dt} + \frac{di_l}{dt}) + R_{arm}(i_u + i_l) \\ + v_{mu} + v_{ml} \end{aligned} \tag{6}$$

$$\begin{aligned} v_{dc1} = L_{arm}\frac{di_u}{dt} + R_{arm}i_u + v_{mu} + L_f\frac{di_s}{dt} \\ + R_{arm}i_s + v_{dc2} \end{aligned} \tag{7}$$

$$v_{ml} + L_{arm}\frac{di_l}{dt} + R_{arm}i_l = L_f\frac{di_s}{dt} + R_{arm}i_s + v_{dc2} \tag{8}$$

III. Reduce Order Model development of The M2DC

The objectives of the Reduced Order Model is to produce a model representing the M2DC seen from each DC side. Therefore, it is possible to make the following assumptions. The model development will be based on the fact that the circulating currents are still remain into the converter and the power balancing between arms is correctly carried out. In this case the AC components will be neglected.

Due to the asymmetry of the converter and based on these assumptions, the following equation could be considered:

$$\begin{aligned} v_{Ctotu} = \langle v_{Ctotu} \rangle &= V_{Ctot} \\ v_{Ctotl} = \langle v_{Ctotl} \rangle &= \frac{V_{Ctot}}{k} \end{aligned} \tag{9}$$

Where k is the arm voltage design ratio.

A. DC1 Side ROM

In this part, based on the Kirchhoff's laws the DC1 side ROM can be developed. We can define the differential current based on the following equations:

$$i_{dc_1} = i_u = i_l + i_{dc_2} \tag{10}$$

Based on (10), we could define the differential current like :

$$\begin{aligned} i_{diff} &= \frac{i_u + i_l}{2} \\ i_{dc_1} &= i_{diff} + \frac{i_{dc_2}}{2} \end{aligned} \tag{11}$$

And therefore

$$v_{dc1} = 2L_{arm}\frac{di_{diff}}{dt} + 2R_{arm}i_{diff} + v_\Sigma \tag{12}$$

with

$$v_\Sigma = v_{mu} + v_{ml} \tag{13}$$

Introducing in (13), (9), it result the following equation:

$$v_\Sigma = m_u.V_{Ctot} + m_l\frac{V_{Ctot}}{k} = m_\Sigma.V_{Ctot} \tag{14}$$

Based on (12) and (11), it could be possible to extend the equations to a M2DC with N legs in (15) to (18).

$$i_{dc_1} = i_{diff_\Sigma} + \frac{i_{dc_2}}{2} \quad \text{with} \quad i_{diff_\Sigma} = \sum_{j=1}^{N} i_{diff_j} \tag{15}$$

$$v_{dc1} = L_1\frac{di_{diff_\Sigma}}{dt} + R_1 i_{diff_\Sigma} + v_{mdc1} \tag{16}$$

with

$$L_1 = \frac{2L_{arm}}{N}; R_1 = \frac{2R_{arm}}{N} \tag{17}$$

$$v_{mdc1} = \sum_{j=1}^{N} \frac{v_{\Sigma_j}}{N} \quad \text{and} \quad m_{dc1} = \sum_{j=1}^{N} \frac{m_{\Sigma_j}}{N} \tag{18}$$

where v_{mdc1} is two time the average value of the v_{diff_j} of each legs and represent the equivalent modulated voltage seen by the DC1 grid. It is link tho the V_{Ctot} voltage by the DC1 equivalent modulation ratio m_{dc1}.

And therefore

$$i_{mdc1} = m_{dc1} i_{diff_\Sigma} \tag{19}$$

From equations (16) to (18), the generalized Reduce Order Model of the DC1 side is as presented in fig. 3.

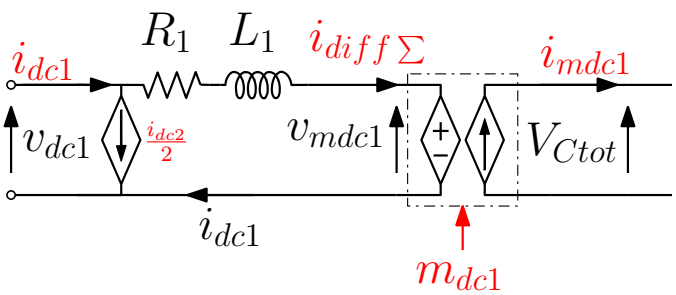

Fig. 3. DC1 side Reduce Order Model Schematic of the M2DC.

As shown in (16), (18), and highlighted in the fig. 3, the current flowing in the secondary DC grid has a direct impact on the DC1 side current. It induce a direct coupling between the two DC grid. This coupling is a major difference with the MMC ROM model [11].

B. DC2 Side ROM

By adding (7) and (8) and considering (5), it is possible to show the relation of the system on the DC2 grid.

$$\begin{aligned} \frac{v_{dc1}}{2} - v_{dc2} = &\left(\frac{L_{arm}}{2} + L_f\right)\frac{di_s}{dt} \\ &+ \left(\frac{R_{arm}}{2} + R_f\right) i_s + v_s \end{aligned} \tag{20}$$

with

$$v_s = \frac{v_{mu} - v_{ml}}{2} \tag{21}$$

Introducing in (21), (9), results in the following equation:

$$v_s = \frac{m_u.V_{Ctot} - m_l \frac{V_{Ctot}}{k}}{2} = m_s.V_{Ctot} \tag{22}$$

Based on (20) and (5), it could be possible to extend the equations to a M2DC with N legs in (23) to (26).

$$i_{dc_2} = \sum_{j=1}^{N} i_{s_j} \tag{23}$$

$$\frac{v_{dc1}}{2} - v_{dc2} = L_2 \frac{di_{dc2}}{dt} + R_2 i_{dc2} + v_{mdc2} \tag{24}$$

$$L_2 = \frac{\frac{L_{arm}}{2} + L_f}{N}; R_2 = \frac{\frac{R_{arm}}{2} + R_f}{N} \tag{25}$$

$$v_{mdc2} = \sum_{j=1}^{N} \frac{v_{s_j}}{N} \quad \text{and} \quad m_{dc2} = \sum_{j=1}^{N} \frac{m_{s_j}}{N} \tag{26}$$

where v_{mdc2} is the average value of the v_{s_j} of each legs and represent the equivalent modulated voltage seen by the DC2 grid. It is link to the V_{Ctot} voltage by the DC2 equivalent modulation ratio m_{dc2}. And therefore

$$i_{mdc2} = m_{dc2} i_{dc2} \tag{27}$$

From equations (23) to (26), the generalized Reduce Order Model of the DC2 side is as presented in fig. 4.

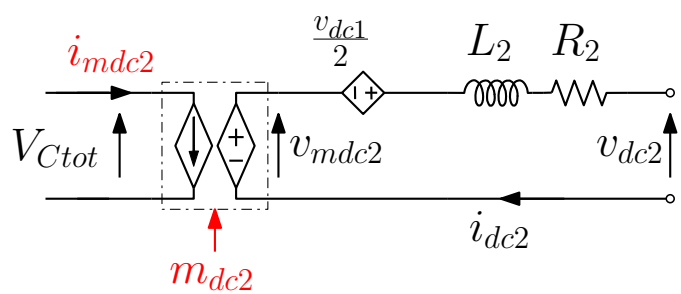

Fig. 4. DC2 side Reduce Order Model Schematic of the M2DC.

C. Internal equivalent M2DC capacitor

A capacitor storage element is linking both sides. This one is linked by all arms equivalent capacitors C_{tot}. to finish building the Reduce Order Model of the M2DC, it is necessary to define the value of internal equivalent M2DC capacitor.

Based on (2), it is possible to estimate the power injected in the equivalent capacitor for a M2DC with one leg. By adding this equation applied on the upper arm and to the lower one divide by k, it is possible to obtain the following equation:

$$C_{totu}\frac{dv_{Ctotu}}{dt} + \frac{C_{totl}}{k}\frac{dv_{Ctotl}}{dt} = m_u.i_u + \frac{m_l}{k}.i_l \tag{28}$$

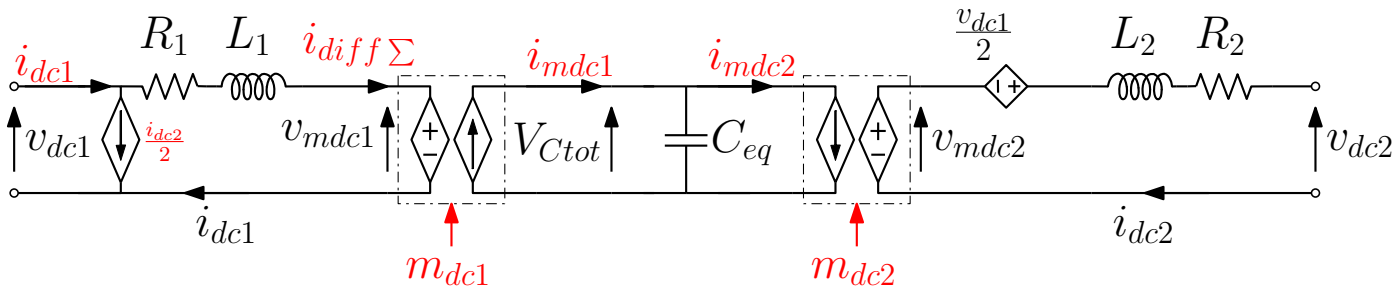

Fig. 5. Reduce Order Model of the M2DC.

Since

$$\begin{aligned} i_u &= i_{diff} - \frac{i_s}{2} \\ i_l &= i_{diff} + \frac{i_s}{2} \end{aligned} \tag{29}$$

Therefore it is possible to develop the following one:

$$\begin{aligned} (C_{totu} + C_{totl})\frac{dV_{Ctot}}{dt} &= (m_u + \frac{m_l}{k}).i_{diff} \\ &+ (-m_u + \frac{m_l}{k}).\frac{i_s}{2} \end{aligned} \tag{30}$$

therefore (30) becomes:

$$(C_{totu} + C_{totl})\frac{dV_{Ctot}}{dt} = m_\Sigma.i_{diff} - m_s.i_s \tag{31}$$

Based on (31), it could be possible to extend the equations to a M2DC with N legs in (15) to (18).

$$\begin{aligned} N(C_{totu} + C_{totl})\frac{dV_{Ctot}}{dt} &= m_{dc1}.i_{diff\Sigma} - m_{dc2}.i_{dc2} \\ C_{eq}\frac{dV_{Ctot}}{dt} &= i_{mdc1} - i_{mdc2} \end{aligned} \tag{32}$$

Therefore, the equivalent capacitor C_{eq} for a M2DC with N legs is equal to N times the sum of C_{totu} with C_{totl}. These equations allow to link the diagrams propose in Fig. 3 with fig. 4 by the equivalent capacitor and gives the ROM of the M2DC shown in fig. 5.

IV. Design of the Control of the M2DC Reduce Order Model

To use and study this reduced model in a large network analysis, it is necessary to enslave the state variables of the latter, namely $i_{diff\Sigma}$, i_{dc2} and V_{ctot}. This part aims to develop the ROM control of the M2DC converter. It will be decomposed into the current control independently and to end on the V_{ctot} control.

A. DC1 current control

From the equation (16) and the Fig. 3, it is possible to edit the Laplace block modeling of the DC1 Side of the M2DC ROM. This model is presented in the upper part of the Fig. 6. Based on the inversion based rules, it is therefore possible to design the control of $i_{diff\Sigma}$ with a PI controller due to the DC nature of this current. This control scheme is presented in the lower part of Fig. 6. In these control, i_x * is the reference of the current i_x.

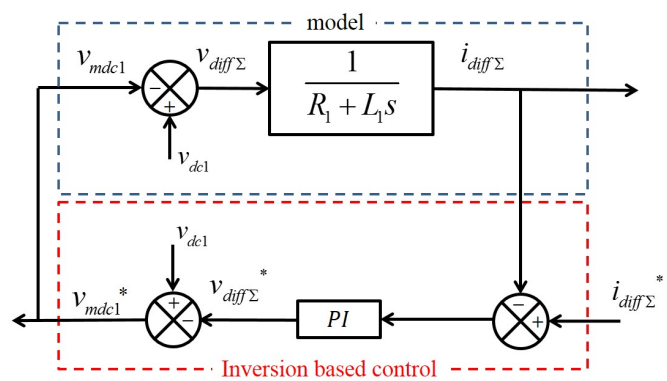

Fig. 6. Control of the M2DC ROM for the DC1 side.

B. DC2 current control

From the equation (24) and the Fig. 4, it is possible to edit the Laplace block modeling of the DC2 Side of the M2DC ROM. This model is presented in the upper part of the fig. 7. as previously, The design of the i_{dc2} control with a PI controller is possible. This control scheme is presented in the lower part of Fig. 7.

C. Control of the Internal equivalent M2DC capacitor voltage

The control of the energy stored in the capacitor C_{eq} can be modeled by (33).

$$\frac{C_{eq}}{2}\frac{dV_{Ctot}}{dt} = p_{dc1} - p_{dc2} \tag{33}$$

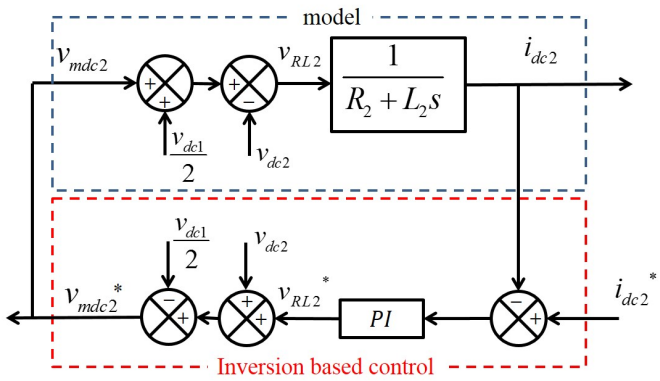

Fig. 7. Control of the M2DC ROM for the DC2 side.

With (15), it is possible to split the p_{dc1} into parts link to $i_{diff\Sigma}$ and i_{dc2}. therefore, (33) become :

$$\frac{C_{eq}}{2}\frac{dV_{Ctot}}{dt} = v_{dc1}.i_{diff\Sigma} - (v_{dc2} - \frac{v_{dc1}}{2}).i_{dc2} \quad (34)$$

The control of the energy stored in the capacitor C_{eq} could be done by $i_{diff\Sigma}$ or by i_{dc2}. As in the literature [7], this paper propose to control it with the $i_{diff\Sigma}$ to have the possibilities to compare both results.

From the equation (34), it is possible to edit the Laplace block modeling of the equivalent capacitor stored energy. This model is presented in the upper part of the Fig. 8. Based on the inversion based rules, it is possible to design the control of V_{ctot}. This control scheme is presented in the lower part of fig. 8.

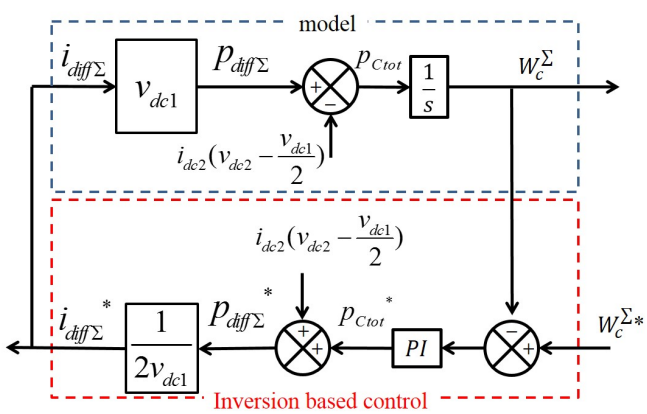

Fig. 8. Control of the equivalent capacitor stored energy of the M2DC ROM.

V. Simulation Results

The M2DC ROM model and its control are validated in this part with parameters summarized in the table I.

TABLE I
M2DC simulation parameters

P_N = 600MW	V_{dc1} = 320kV	V_{dc2} = 250kV
N = 3	f_s = 300 Hz	k = 1.1
L_{arm} = 10mH	R_{arm} = 10mΩ	V_{Ctotu} = 320 kV
L_f = 100mH	R_f = 100mΩ	V_{Ctotl} = 290 kV

To validate the value of the equivalent capacitor C_{eq}, a first simulation was carried out for the M2DC as presented in [7] and the proposed ROM model with the energy control deactivated. The results are shown in Fig. 9. At t=50ms, a step from 0W to P_N has been performed on p_{dc1} generating an increase in the energy stored in the capacitor of the converter. At t = 200ms, a step from 0W to P_N was performed on p_{dc2} rebalancing the power on each side and stopping the increase in the energy stored in the converter. This simulation validate firstly the correct model of the DC1 and 2 sides since currents and powers are equal between the ROM model (ROM) results and the Electromagnetic transient (EMT) one. The value of C_{eq} is validated since the evolution of the average value of V_{Ctot} are the same for both model.

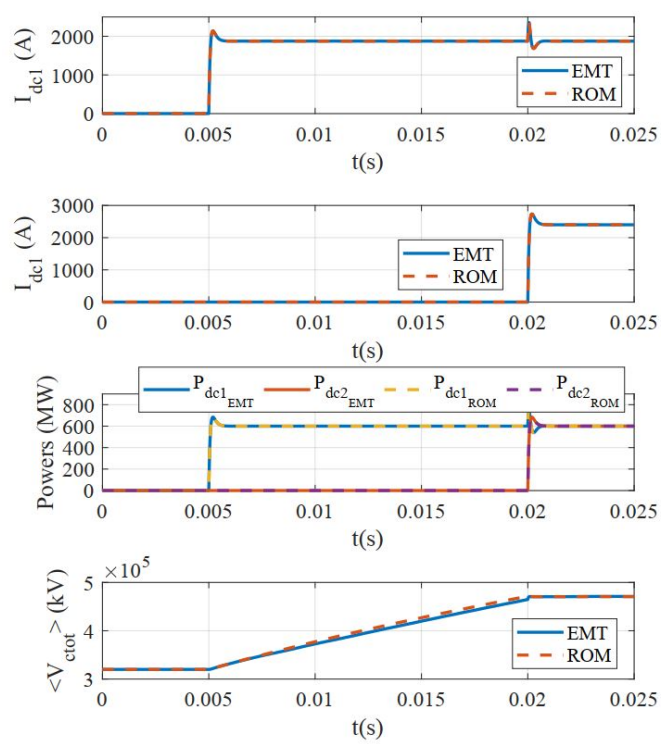

Fig. 9. C_{eq} and DC sides model validation

The control of energies in a second time is validated by generating firstly a step on p_{dc2} from 0W to P_N, as

shown in fig 10, i_{dc2} and the i_{dc1} will generate a step to regulate the V_{Ctot} at the correct value. In a second time, a step is done on the references of V_{Ctot} to 380kV and the i_{dc1} is increasing transiently to store the energy at the correct value. For this simulation, both EMT and ROM simulation give the same results validating the model and the control.

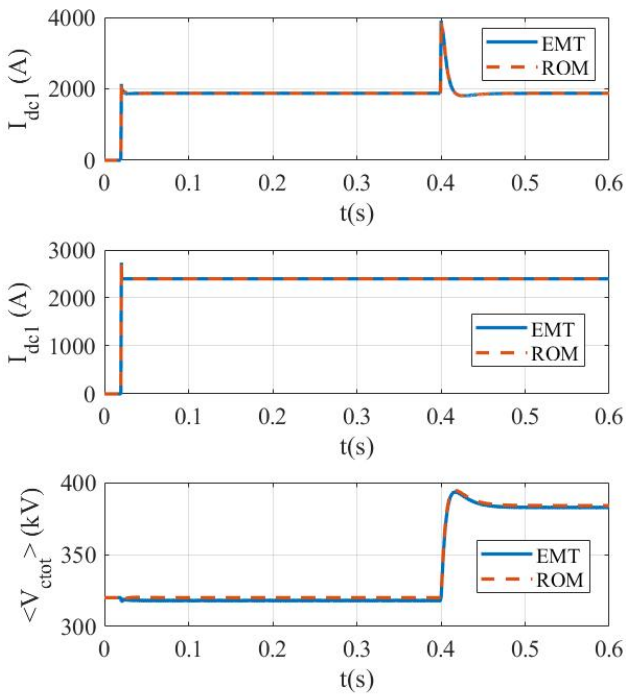

Fig. 10. ROM model and control validation

VI. Conclusion

In order to carry out stability studies of MTDC grid with DC/DC converters, the development of reduce order models is needed. Indeed no reduced model of DC/DC converter for HVDC is available except if the DC/DC topology is based on the MMC topology in AC/DC version like the MMC DAB. This paper propose a reduce order model of the Modular Multilevel DC Converter (M2DC). The paper presents firstly the basics of the M2DC converter. Secondly, the development of the reduce order model has been presented. This model is splitted in three parts, the model development for both DC side independently and lastly the evaluation on the internal equivalent M2DC capacitor. The model developed allows the order to be reduced from 12 to 3. The development of the control of this model is carried out in the third part. The comparison of the reduce order model and its control to the average arm model of the M2DC is performed in the last part of the paper. This last part shows that the developed model preserves the average internal dynamic behaviour of the M2DC and validate the ROM model. This simplified model is suitable for large scale dynamic studies but as it does not take into account the block state behaviour of the M2DC converter, it cannot be used for fault studies. Thus, from this model, the introduction of M2DC into a small signal stability analysis is possible and constitutes the next step of the work to be carried out.

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