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A Simple Carrier-Based Modulation for the SVM of the Matrix Converter

F. Gruson, Ph. Le Moigne, Ph. Delarue, A. Videt, X. Cimetière and M. Arpillière.

Abstract - Today, industry has not fully embraced the matrix converter solution. One important reason is its high control complexity. It is therefore relevant to propose a simpler but efficient modulation scheme, similar as three phase VSI modulators with the well-known symmetrical carrier-based ones. The modulation presented in this paper is equivalent to a particular Space Vector Modulation (SVM) and takes into account harmonics and unbalanced input voltages, with the same maximum voltage transfer ratio (86%). The aim of this work is to propose a simple and general pulse-width-modulation method using carrier-based modulator for an easier matrix converter control. Furthermore, a simple duty cycle calculation method is used, based on a virtual matrix converter. Finally, simulations and experimentations are presented to validate this simple, original and efficient modulation concept equivalent to matrix converter SVM.

Index Terms - Matrix converter, power conversion, AC–AC, AC–AC conversion, power converter, pulse-width-modulated power converters, pulse-width modulation, PWM, DPWM.

I. INTRODUCTION

The Matrix Converter, shown in Fig. 1, is a direct three-phase to three-phase forced-commutated power converter which directly connects the mains power supply (r, s, t) to the motor (u, v, w) through nine fully controlled bidirectional switches. The input network (r-in, s-in, t-in) is connected to the matrix converter through an L–C input filter as shown in Fig. 1. This converter, which can be decomposed in three “cells” as shown in Fig. 1, generates variable frequency and amplitude output voltages (limited to 86% of the input voltage amplitude with over-voltage modulation) with any three-phase electrical network. This converter is able to produce sinusoidal input currents, which limits the volume of the L–C input filter.

This converter has a high power density and a potentially high reliability since electrolytic storage capacitors are not required. Thus, it could become a compact industrial solution for adjustable speed drives feeding induction motors.

![Matrix Converter Scheme](image)

Fig. 1. The Matrix Converter scheme

The more useful and interesting modulations are the Space Vector Modulation (SVM) [1]-[4] and the Rectifier and Inverter Vector Modulation (RIV) [5], [6]. These modulations are based on graphical representation methods, duty cycle calculations, and sequenced states application to create the Pulse-Width Modulation (PWM). An 86% voltage ratio (RMS fundamental output voltage divided by the RMS input voltage) is obtained with these methods. In fact, both modulations are equivalent and able to produce sinusoidal output voltages, even when there is unbalance or harmonics in the mains voltages. Since current references of the mains are chosen proportional to the input voltages, input currents are balanced and sinusoidal as long as the mains power supply is a perfect sinusoidal source. A PWM that limits the number of switchings during the modulation period has also been introduced with the SVM representation, using the calculated duty cycles and a defined switching table [7]-[8]. These matrix converter modulations are efficient, but complex to understand, to synthesize compared to the three phase voltage source inverter (VSI) modulations, and thereby heavy to implement in digital processors. The carrier based modulations proposed in the literature are complex to implement into industrial process, by using a discontinuous carrier wave modulator [9], [10] or an asymmetrical one which needs to sum some duty cycles [11],[12].

Hysteresis control methods and Direct Torque Control (DTC) for matrix converter are other interesting alternatives [1],[13],[14]. However, drawbacks still exist such as torque ripple in the low speed region or switching frequency variation according to the change of the motor speed. Thus, industrial applications still focus on controlled-frequency PWM, and especially carrier-based solutions.

Today, industry has not fully embraced the matrix converter solution, mainly due to its high control complexity (modulation, switching control...) and implementation in a digital processor...
II. SPACE VECTOR MODULATION (SVM) FOR MATRIX CONVERTER

In this part, the basic knowledge of the SVM applied to matrix converter is introduced to highlight the proposed modulation objectives. The well-known matrix converter Space Vector Modulation (SVM) [1]-[4] approach leads to define three vector families:

- First family: 6 rotating vectors (each phase input is connected to a different phase output).
- Second family: 3 null vectors (free wheeling is a switches configuration leading to zero voltage on the load) called \( O_i \) with \( i = 1, 2 \) or 3.
- Third family (the remaining ones): 18 active vectors called \( A_j \) (with a fixed angular position, and proportional to one input phase-to-phase voltage), where \( j \) is an integer between 1 and 18.

Matrix SVM modulations use only the two last families to create output voltages and input currents [17], [18], as the first one has a vector position varying with the time, which is not useful for building the references with the space vector approach.

The general matrix SVM sequence, shown in Fig. 2, uses four active vectors \( A_k \) (among the six vectors nearest to the output voltage reference vector), and one to three null states \( O_i \) to complete the PWM period. This specific sequence allows having only one switching when a vector is changed.

During a PWM period (T) [19]-[21],

The null vector \( O_2 \) automatically involves at the output the common potential to \( U_1 \) and \( U_2 \), which is in fact the highest input phase potential in absolute value. A particular modulation can be defined by only using this null state \( O_2 \), which generates a discontinuous modulation (DPWM) [19]. This terminology is proposed here, as this specific choice allows blocking one of the three “switching cells” of the matrix converter, in the same way as one inverter leg is blocked when using discontinuous PWM in VSI. This particular modulation, presented in Fig. 3, reduces the number of switching and increases the converter efficiency compared to the general SVM sequence (Fig. 2).

III. COMPUTING THE DPWM CONVERSION MATRIX [M]

The calculation method of the conversion matrix [M], involving the DPWM and based on a virtual matrix converter concept, is presented in this part.

In order to avoid any short circuit of the input voltage sources and open circuit output currents, the sum of duty cycles for each cell must be equal to 1:

\[
m_{rk} + m_{sk} + m_{ik} = 1, \quad k \in \{u, v, w\}
\]

A. Conversion matrix [M] calculation

A general relation [16] for producing two output phase-to-phase voltages with the three input phase-to-phase ones is defined in (3). Since the three phase-to-phase voltages are equal to zero, the third output voltage is automatically deducted from (3).

\[
\begin{align*}
    u_{uv} &= b_{rs} \cdot u_{rs} + b_{rt} \cdot u_{rt} + b_{tr} \cdot u_{tr} + b_{rs} \cdot u_{rr} \\
    u_{uw} &= c_{rs} \cdot u_{rs} + c_{rt} \cdot u_{rt} + c_{tr} \cdot u_{tr} + c_{rs} \cdot u_{rr}
\end{align*}
\]

\( b_{ij} \) is a duty cycle that connects \( u_{ij} \) to \( u_{uv} \). Indirectly, \( b_{rs} \) controls the 4 switches that can connect \( r \) or \( s \) to \( u \) or \( v \). \( c_{ij} \) is associated to the output voltage \( u_{uw} \). Since coefficients \( b_{ij} \) and \( c_{ij} \) are duty cycles, they are automatically bounded between zero and one.
With the aim of producing an equivalent modulation to the SVM, only the two largest input phase-to-phase voltages \((U_1\) and \(U_2\)) must be introduced as explained earlier. In order to simplify the calculation of the conversion matrix \([M]\), [16] has proposed to calculate the duty cycles of \([M]\) with particular values of input voltages and output voltage references, as shown in Fig. 4.

\[
\begin{align*}
\text{for } & u_{uv} = m_{sv} \times u_{rs} + m_{rv} \times u_{rt} + m_{rv} \cdot u_{rr} \\
\text{for } & u_{uw} = m_{sw} \times u_{rs} + m_{rw} \times u_{rt} + m_{rw} \cdot u_{rr}
\end{align*}
\]

(4)

As the output potential “u” is always connected to the input phase “r”, the “u” cell is necessarily blocked. The duty cycles used in equation (4) are defined in (5) and derived from [14], considering that:
- all duty cycles are chosen proportional to the input voltage in order to have input current proportional to the input voltage, as explained in the appendix and in [16], [22]-[23].
- The u cell is blocked.

This way, duty cycles and then the conversion matrix \([M]\) can be defined (5). This solution has the advantage of only requesting the calculation of four duty cycles.

\[
[M] = \begin{bmatrix}
1 & 1 & 1 & 1 \\
0 & \frac{(u_{2s} - u_{2r}) \cdot u_{rs}}{u_{rs}^2 + u_{rr}^2 + u_{rt}^2} & \frac{(u_{2s} - u_{2r}) \cdot u_{rt}}{u_{rs}^2 + u_{rr}^2 + u_{rt}^2} & \frac{(u_{2s} - u_{2r}) \cdot u_{rr}}{u_{rs}^2 + u_{rr}^2 + u_{rt}^2} \\
0 & \frac{(u_{1s} - u_{1r}) \cdot u_{rs}}{u_{rs}^2 + u_{rr}^2 + u_{rt}^2} & \frac{(u_{1s} - u_{1r}) \cdot u_{rt}}{u_{rs}^2 + u_{rr}^2 + u_{rt}^2} & \frac{(u_{1s} - u_{1r}) \cdot u_{rr}}{u_{rs}^2 + u_{rr}^2 + u_{rt}^2}
\end{bmatrix}
\]

(5)

In the case of asymmetric components and/or harmonics contained in input voltages, the matrix \([M]\) defined in (5) automatically compensates input voltage disturbances [17]. This property will be presented and validated in the simulation of the conversion matrix part (III.C).

### B. Matrix-Based Type

The \([M]\) matrix defined in (5) is simple to compute but cannot be used directly for all input and output voltages values. This section defines how this principle can be extended to obtain \([M]\) in any case.

In order to use always the greatest matrix converter input phase-to-phase voltages and to block one of the three switching cells, it is necessary to permanently connect the greatest absolute input voltage to the greatest output voltage with the same sign as the input one, as showed in Fig. 5. This way, the modulation is created by the variation of the two other output potentials which have to be sorted in value and sign (+, 0, 0+, 0, -), with:
- +: highest potential
- 0: intermediary potential, with a positive value (0+), with a negative value (0-)
- -: lowest potential

![Fig. 5. The 2 possibilities of classified voltage](image)

The choice of the blocked switching cell and of its “ON switch” is dependent on the greatest values of the input voltages (r, s, t) and of the output voltage references (u, v, w), which changes with the time. Two selectors (Fig.6.) have been introduced to realize these inputs and outputs voltage classifications.

In order to be able to use at any time the same matrix-based duty cycle (5), a “virtual matrix converter” (Fig. 6) is introduced with classified input (r’, s’ and t’) and output (u’, v’ and w’) made by both selectors. This virtual converter always has its first virtual cell (u’ cell) blocked as shown in Fig. 6. Consequently, the duty cycle \(m_{rs'}\) is always equal to 1, and other duty cycles of the first cell (\(m_{rs'}\) and \(m_{rv'}\)) are always equal to zero.

![Fig. 6. Virtual matrix converter concept with its two selectors](image)
can be classified, with “+” defining the greatest, “-” the lowest and “0” the intermediary one. Thus, selectors have been defined with the following principles:
- The aim of the input selector is to connect the two positive and greatest input phase-to-phase voltages to \((r', s')\) and \((r', t')\) inputs of the virtual converter. For this, the input potential with the largest absolute input value (input potential with the opposite sign to the other two) is always connected to \(r'\).
- The output selector connects to \(u\) the output which has the largest voltage reference with the same sign as \(r'\) input,
- This modulation method needs to compute, at any moment, the same four duty cycles \(m_{s',v'}, m_{w',v'}, m_{s',w'}\) and \(m_{s',w'}\), using equation (4) as shown in (6). The two other input potential assignments \((s'\) and \(t'\) assignment) and two last columns (for \(v'\) and \(w'\) assignment) in the conversion matrix \(\text{[M}_{\text{Virtual}]\) defined in (6). A choice has been done to be able to determine the conversion matrix \([M]\).

\[
\begin{bmatrix}
    m_{v',s} = l & m_{v',w} = l - m_{v',w} = m_{s',v} - m_{v',w} = l - m_{v',w} = m_{s',v} \\
    m_{v',s} = 0 & m_{v',w} = \frac{u_{v',s} - u_{v',w}}{u_{v',s} + u_{v',w}} = \frac{u_{v',s} - u_{v',w}}{u_{v',s} + u_{v',w}} \\
    m_{v',w} = 0 & m_{v',w} = \frac{u_{v',w} - u_{v',s}}{u_{v',w} + u_{v',s}} = \frac{u_{v',w} - u_{v',s}}{u_{v',w} + u_{v',s}}
\end{bmatrix}
\]  

(6)

The final conversion matrix \([M]\) is defined by relation (7).

\[
[M] = [M_{Input\,Selector}] \times [M_{Virtual}] \times [M_{Output\,Selector}]
\]  

(7)

Finally, the conversion matrix \([M]\) is obtained with a lines and columns specific rotation of the virtual converter conversion matrix \([M_{Virtual}]\).

C. Simulations of the conversion matrix

This method for generating the conversion matrix \([M]\) has been implemented in Matlab-Simulink\textsuperscript{®} software. Fig. 7 shows the matrix converter input and output voltages and currents without PWM with a 50-Hz input frequency and maximal voltage input network equal to 325V. The output reference is created with 30Hz and 195V maximal voltage values. The matrix converter operates at 10kVA R-L load with a power factor of 0.86 (4.9Ω; 15.5mH). The 195V at 30Hz voltage applied to this three phases load generates a 34.2A maximum value of the output currents. In order to conserve the input and output active power equality, the maximal input currents should be equal to 17.6A. Fig. 7 validates this modulation approach as the electrical outputs and inputs have the expected values.

Fig. 7. Simulation of the matrix converter with the average model
(a) Input network voltages (imposed by the grid)
(b) Input network currents generated by the modulation
(c) Output voltages generated by the modulation
(d) Output currents generated in the R-L load
Fig. 8 shows the \(u\) cell duty cycles \(m_{s'}, m_{s'}, m_{s'}\). One of these three duty cycle is equal to one and the two others to zero when \(V_{rn'}\) is the largest output reference with the same sign as the largest absolute input voltage, which illustrates the DPWM.

Fig. 8. Simulation of the matrix converter with average model
(a) Input network voltages (imposed by the grid)
(b) Output voltages generated by the modulation
(c) 3 duty cycle evolution in the “u cell” of the matrix converter

This modulation has also been successfully validated by simulation with variable input and output constraints (variations of the frequency, of the input voltages and variable voltage transfer ratio limited to 86%), and under unbalanced/disturbed conditions. Fig. 9 shows simulation results of the proposed modulation in this case. One input voltage is increased by 10% and an homopolar component is added in the network voltage (5% of the rms network voltage at 500Hz). The output reference is created with 30Hz and 195V values. The matrix converter operates at 10kVA R-L load with a power factor of 0.86.
Assignment strategy

IV. MATRIX CONVERTER PWM MODULATOR

These nine duty cycles \( m_k \) have to be transformed into logical signals adapted for the control of the nine switches \( S_k \), generating the connection matrix \([S]\) \( (8)\), with the help of a carrier-based PWM.

\[
[S] = \begin{bmatrix}
S_{ru} & S_{rv} & S_{ru} \\
S_{su} & S_{sv} & S_{ru} \\
S_{tu} & S_{tv} & S_{ru}
\end{bmatrix}
\] \( (8)\)

A. Carrier Based Switching Cell Modulator.

Each switching cell (u, v, w) is composed of three switches, with only one “ON” switch in each cell at any time \( (9) \).

\[
S_{ru} + S_{su} + S_{tu} = 1 \\
S_{rv} + S_{sv} + S_{tv} = 1 \\
S_{rw} + S_{sw} + S_{tw} = 1
\] \( (9)\)

With \( S_{ij}=1 \) when the switch \( S_{ij} \) is ON, \( S_{ij}=0 \) when it is OFF.

The principle of the modulator, for each switching cell, is to compare one duty cycle to a triangle carrier wave and a second one to this carrier wave complemented to 1. The logic control of the last switch is created by the complement to 1 of the sum of the two previous logic signals as shown in Fig. 10.

B. Matrix Converter Carrier-Based Modulator

In order to reproduce the DPWM SVM modulation, each duty cycle of a matrix line must be assigned in “real time”, with the help of “selector concept” \( (\text{Fig. 6}) \), to the same control allocation \( \text{(comparison to the carrier wave, to its complement to 1 or equal to the sum of both previous duty cycles complemented to 1)} \). According to “ON signal” positions \( \text{(Fig. 10)} \), it can be noted that the line complemented to one creates the “ON” state automatically in the “medium part” of each slope, similarly to the position of the null vector \( O_2 \) in the DPWM SVM modulation \( \text{(Fig. 3)} \).

The null vector \( O_2 \) line in the DPWM SVM modulation must be detected in the conversion matrix \([M]\). It is necessarily the one with a duty cycle equal to 1 (blocked cell). Then, to the two other lines must be assigned to carriers as shown in Fig. 11. Therefore, the control allocation changes during time (“selector concept”). In example \( \text{(Fig. 12)} \), the second line has the duty cycle equal to one \( (m_{s2}) \). Therefore the carriers control is affected here to the first and third lines. Fig. 12 also illustrates both the active vectors \( A_k \) and the null vector \( O_2 \), connected here to the “s” input. The second cell \( (v \text{ cell}) \) is blocked (DPWM) and is always connected to the “s” input.

Assignment strategy

![Assignment strategy](image)

Fig. 10. The based switching cell modulator \( \text{(ex where } S_{su} \text{ is complemented)} \)

According to this description, the ON switching signal created by the “sum complement to 1” appears automatically in the middle of each slope \( (S_{su} \text{ in Fig. 10)} \), and the other ON switch signals, at the beginning and the end of the carrier slope \( (S_{m} \text{ and } S_{ru} \text{ in Fig. 10)} \).

\[
[M] = \begin{bmatrix}
m_{ru} & m_{rv} & m_{ru} \\
m_{su} & m_{sw} & m_{ru} \\
m_{tu} & m_{tv} & m_{ru}
\end{bmatrix}
\]

Fig. 11. “Real time” Concept of Matrix duty cycle line assignment.
This carrier-based modulator is simple to implement and needs only the calculation of the four duty cycles of $[M]$. It can be applied, with same results, on the virtual converter or on the real matrix converter (Fig. 13) according to the good choice of the line “complemented to one”. The output of modulator is the connexion matrix $[S]$.

This feature allows making a more flexible modulator and facilitates its implementation in an industrial application.

### C. Simulations

This carrier-based modulator has been implemented in Matlab-Simulink® software with the same balanced conditions as in the previous part and with a 10-kHz carrier wave frequency. This modulation technique has been compared to the classical SVM modulation and gives the same value of the connexion matrix $[S]$ for both modulations in each sampling time. Fig. 14 shows the DPWM simulation of the matrix converter. As they are chopped sinusoidal voltage at 30Hz, the output voltage ($v_{un}$) is shown in continuous bold line.

Fig. 15 shows simulation results of one output voltage ($v_{ur}$) and the common mode voltage $v_{un}$. The $v_{un}$ voltage illustrates the blocking state (DPWM) of the “u cell” when $v_{urn}$ is the largest output reference, with the same sign as the largest absolute input voltage.

### V. Experimentation

A matrix converter prototype as shown in Fig. 16 has been developed with FF200R12KT3_E IGBT and ARCAL2210 driver modules to test this original modulation method, implemented here to a DSP from Texas Instrument (TMS320F2812) and a CPLD from Altera (DB3256-144).

The matrix converter input filter is composed of a 0.6mH inductor, which has a 4.7mΩ internal resistance, and a 10μF capacitor. Experimental results shown in the Fig.17 to Fig.19 have been obtained with an input voltage equal to 120V RMS at 50Hz. The matrix converter has been connected to a three phases R-L load with a 0.63 power factor (R=11.85Ω; L=7.7mH). The ratio q (RMS output voltage divide by the RMS input voltage) is set to 0.8, the output voltage is 96V RMS and the output frequency is defined at 30Hz. The triangle carrier wave frequency has been set to 10 kHz.

For secure commutations, gate transistor signals of Matrix...
converter require proper sequences as presented in [4],[24]-[27]. The commutation sequence used in our experiment is either two step current commutation sequences technique or four step voltage commutation sequences ones. A clamp circuit [1],[25] has also been introduced in the matrix converter prototype, as a safety system, in order to prevent any commutation failure.

The input and output power are approximately equal to 925W. These input and output waveform allows validating the operation of the proposed matrix converter modulation.

VI. CONCLUSION

This paper has presented an original carrier-based modulator for matrix converters based on a “virtual matrix converter” concept. The proposed modulation concept is illustrated with the DPWM which blocks one of the three switching cell. This choice limits to four the number of duty cycle calculations. The proposed carrier-based modulator creates the same instantaneous connexion matrix [S] as the SVM or the RIV (in the DPWM specific case here), but with less calculation and with a more synthesized and systematic approach. Therefore, this modulation is easier to implement compared to the previous ones and has been patented [28], [29].

Furthermore, the basic modulation concept, illustrated in this paper with the DPWM, can be extended in a simple way to other modulation choices. A future paper will present the general modulation process taking into account the different null states possibilities (freedom degrees) in order to obtain better converter performances (losses, EMC, input currents and output voltages THD…). Afterwards, it should be an interesting work to compare the efficiency and the electrical characteristics of the proposed modulation methods with the DTC modulation. Then, we should get a global overview of matrix modulation solutions and performances for industry applications.

Finally, the proposed modulation cannot tune the input power factor. In future work, it would be an interesting trend to introduce this parameter in the proposed method to be able to compensate the slight phase shift introduced by the L-C input filter between voltage and current [30] and/or generate reactive power flow for ancillary services in electrical grid (wind turbine applications…).
APPENDIX

The input currents are chosen to be in phase with their respective input voltages. Each input current is proportional to the respective input voltage. The input reactive power must be null as shown in (10).

\[
\begin{align*}
    i_r \quad &= \quad N \frac{v_{rn}}{v_{sn}} \quad = \quad \frac{v_{rn}}{v_{sn}} \\
    i_s \quad &= \quad \frac{p}{v_{rn}^2 + v_{sn}^2 + v_{in}^2} \\
    i_u \quad &= \quad \frac{\alpha \cdot u_{rs}}{v_{rn}^2 + v_{sn}^2 + v_{in}^2} \\
    i_c \quad &= \quad \frac{\beta \cdot u_{rs}}{v_{rn}^2 + v_{sn}^2 + v_{in}^2}
\end{align*}
\]

(10)

We can define (11) by the general matrix Kirchhoff’s laws

\[
\begin{align*}
    i_r \quad &= \quad [M] \times i_s \\
    i_s \quad &= \quad \left[ \begin{array}{c} m_{rs} \\ m_{rs} \\ m_{rs} \end{array} \right] \\
    i_u \quad &= \quad \left[ \begin{array}{c} m_{rs} \\ m_{rs} \\ m_{rs} \end{array} \right]
\end{align*}
\]

(11)

In this example the \( i_c \) current is detailed and leads to relation (12).

\[
\begin{align*}
    i_r \quad &= \quad \frac{p \times v_{rn}}{v_{rn}^2 + v_{sn}^2 + v_{in}^2} = \alpha_r \times p \\
    i_s \quad &= \quad m_{rs} i_r + m_j i_s + m_{rs} i_u
\end{align*}
\]

(12)

The input power must be equal to the load power since no storage is used on the matrix converter.

\[
\begin{align*}
    i_r \quad &= \quad \alpha_r (v_{sn} \times i_u + v_{sn} \times i_r + v_{sn} \times i_u) \\
    i_u \quad &= \quad m_{rs} i_r + m_j i_s + m_{rs} i_u
\end{align*}
\]

(13)

The easiest solution for the equation (13) is shown in (14).

\[
\begin{align*}
    m_{rs} \quad &= \quad \alpha_r \times v_{sn} = \frac{v_{rn}}{v_{rn}^2 + v_{sn}^2 + v_{in}^2} = K \times v_{sn} \\
    m_{rs} \quad &= \quad \alpha_r \times v_{sn} = \frac{v_{rn}}{v_{rn}^2 + v_{sn}^2 + v_{in}^2} = K \times v_{sn} \\
    m_{rs} \quad &= \quad \alpha_r \times v_{sn} = \frac{v_{rn}}{v_{rn}^2 + v_{sn}^2 + v_{in}^2} = K \times v_{sn}
\end{align*}
\]

(14)

A simple and evident solution to define switches duty cycles is to have proportionality with input voltages. The calculation method [5] uses the phase-to-phase voltage. This proportionality must be verified with the combination switches duty cycles (\( b_{ij}, c_{ij} \)).

\[
\begin{align*}
    b_{rs} \quad &= \quad \frac{b_{rs} \cdot u_{rs} + b_{rs} \cdot u_{rs} + b_{rs} \cdot u_{rs}}{u_{rs} + u_{rs} + u_{rs}} \\
    c_{rs} \quad &= \quad \frac{c_{rs} \cdot u_{rs} + c_{rs} \cdot u_{rs} + c_{rs} \cdot u_{rs}}{u_{rs} + u_{rs} + u_{rs}}
\end{align*}
\]

(15)

The \( u_{rs} \) voltage can be decomposed into three input voltages and switch duty cycles.

\[
\begin{align*}
    u_{rs} \quad &= \quad (m_{rs} \cdot v_{rn} + m_{rs} \cdot v_{sn} + m_{rs} \cdot v_{in}) \\
    u_{rs} \quad &= \quad (K \cdot v_{rn}^2 + K \cdot v_{sn}^2 + K \cdot v_{in}^2) \\
    u_{rs} \quad &= \quad (K \cdot v_{rn}^2 + K \cdot v_{sn}^2 + K \cdot v_{in}^2) \\
    u_{rs} \quad &= \quad (K \cdot v_{rn}^2 + K \cdot v_{sn}^2 + K \cdot v_{in}^2)
\end{align*}
\]

(16)

The easiest solution for equations (15) and (16) is shown in (17).

\[
\begin{align*}
    b_{rs} \quad &= \quad \alpha \cdot u_{rs} \\
    c_{rs} \quad &= \quad \beta \cdot u_{rs}
\end{align*}
\]

(17)

It is therefore possible to conclude that switch duty cycles combination (\( b_{ij}, c_{ij} \)) can be proportional to their input phase-to-phase voltage.

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Biographies

François Gruson received the Ph.D. degree in electrical engineering from the Ecole Centrale de Lille, Lille, in 2010. Since 2011, he has been working as Associate Professor at Arts and Metiers ParisTech in the Laboratoire d’Electrotechnique et d’Electronique de Puissance of Lille (L2EP), Lille, France. His research interests include direct AC-AC converter especially matrix converter for adjustable-speed drives, power quality and power electronic converter for electrical grid application.

Philippe Le Moigne (M’93) received the Engineering degree from the Institut Industriel du Nord, Lille, France, in 1986 and the Ph.D. degree in electrical engineering from the University of Lille, in 1990. He is currently a Professor with the Laboratoire d’Electrotechnique et d’Electronique de Puissance, Ecole Centrale de Lille, where he is also the Head of the Power Electronics Department. His major fields of interest include hard switched power converters and supercapacitors, especially the control of multilevel and matrix topologies for medium- and high-power applications with the aim of high power quality and high efficiency.

Philippe Delarue received the Ph.D. degree from the University of Sciences and Technologies of Lille, Villeneuve d’Ascq, France, in 1989. Since 1991, he has been an Assistant Professor with the Polytech’Lille and the Laboratory of Electrotechnics and Power Electronics, Ecole Polytechnique, Université de Lille, Villeneuve d’Ascq. His main research interests include power electronics and multimechanic systems.

Arnaud Videt received the Ph.D degree in electrical engineering from the Ecole Centrale de Lille, Lille, France. Since 1992, he has been a Research Engineer with the Laboratoire d’Electrotechnique et d’Electronique de Puissance, Ecole Centrale de Lille, Lille. His current research interests include power electronics and the control of electric machines.

Xavier Cimetière received the Engineering degree from Ecole Centrale de Lille, Lille, France. Since 1982, he has been a Research Engineer with the Laboratoire d’Electrotechnique et d’Electronique de Puissance, Ecole Centrale de Lille, Lille. His research interests include power electronics and the control of electric machines.

Michel Arpilliere was born in Paris, France, in 1952. He received the M.S. degree in physics and math from Paris VII University, Paris, France. He is a Senior Power Electronics Research/Design Engineer in Schneider Electric, a worldwide French company, which is involved in the broad electrical business. He has been working in the Schneider Drive Department for more than 20 years, after several years spent in a small Switch Mode Power Supply (SMPS) company. He is presently “Drive Architect” in Schneider Toshiba Inverter, and a member of the board the European Center of Power Electronic.