Energy and Director Switches Commutation Controls for the Alternate Arm Converter

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Abstract

The Alternate Arm Converter (AAC) is promising multilevel Voltage Source Converter (VSC) suitable for High Voltage Direct Current (HVDC) transmission systems. This converter exhibits interesting features such as a DC Fault Ride Through capability thanks to the use of Full-Bridge Sub-Modules (SM) and a smaller footprint than an equivalent Modular Multilevel Converter (MMC).
After an analysis of the converter operating modes called Non-overlap and Overlap mode, a sequential representation of the AAC operation is proposed. The main originality of this paper is the use of the Petri Net to describe all the phases and to highlight their sequencing. According to the phases identified thanks to the sequential approach, models and control structures for the grid currents, the internal energy and the Zero Current Switching (ZCS) are detailed. Furthermore, the step-by-step approach proposed in this paper allows a clear and rigorous modelling of this complex converter.

Keywords: High Voltage Direct Current; Voltage Source Converter; Multilevel Converters; Control

1. Introduction

Multilevel converters have become recently a suitable solution for new HVDC transmission systems. Historically, AC grids with different characteristics were interconnected by Line Commutated Converters (LCC) based HVDC links. LCCs are very high power and efficiency converters however they suffer of a poor energy quality. Original VSC topologies like the 2-level converter could not be considered for high power links due to the large number of the serial connected Insulated Gate Bipolar Transistors (IGBT) and the losses generated by high frequency Pulse Width Modulation (PWM).

Over the last two decades, advances in power electronics technology fostered the generation of new multilevel VSC topologies to be used in recent and upcoming HVDC links. Presently, the reference topology for VSC-HVDC is Modular Multilevel Converter (MMC). The MMC topology published in [1] has been largely studied during these 5 last years and is considered as a real technological breakthrough in VSCs for HVDC transmission systems. Nowadays, Half-bridge (HB) MMCs are already used in some point-to-point links such as the INELFE Link which uses four MMCs to transmit up to 2GW in two parallel cables. This topology has several attractive features as a higher power capability than 2-level VSC, high frequency carrier based PWM to generate high quality AC currents is not needed anymore as several voltage levels are available and the passive filters are almost totally removed. Moreover, the MMC has an excellent efficiency (>99%)[2] when it is composed of HB SMs. Nonetheless, the inability of HB SMs to generate negative voltage levels renders the converter unable to oppose the AC grid voltage during DC-side fault, leading to highly destructing in-rush fault currents. Thereby research efforts have been made to propose either, MMC with different SM topologies allowing a DC-Fault tolerance while limiting the impact on power losses [3, 4, 5] or new multilevel VSC topologies.

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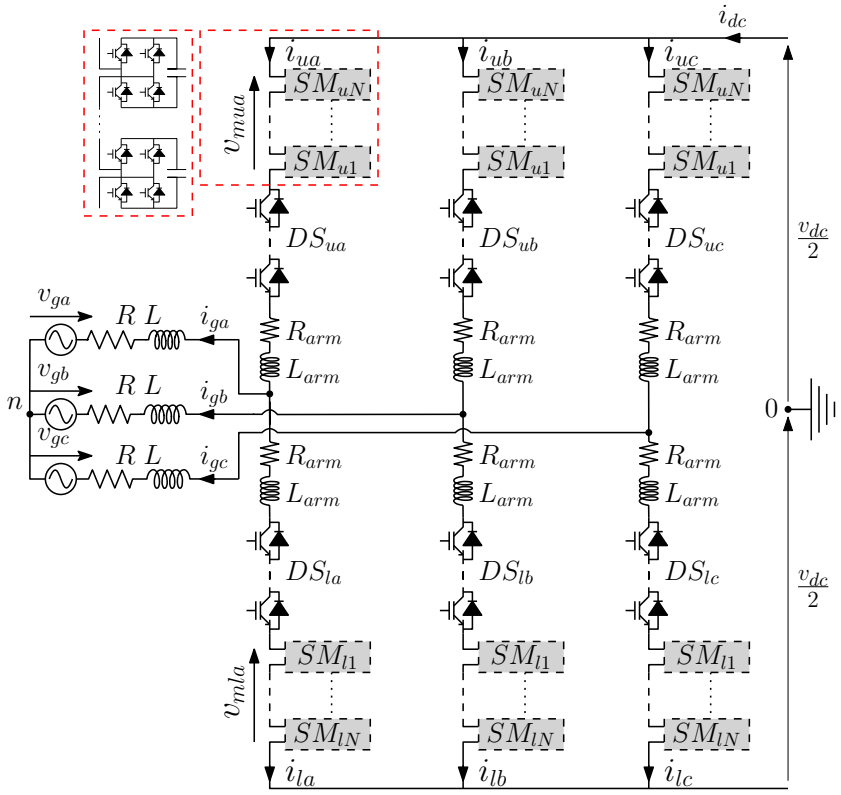

Figure 1: Alternate Arm Converter scheme

One of these new topologies of VSC-HVDC with DC-Fault blocking capability is the Alternate Arm Converter which has been first published in 2010 [6]. The aim of this topology is to take the main strengths of the MMC and to improve the other features such as the DC-Fault tolerance and the converter footprint [7, 8]. The converter is composed of three legs, six arms and each arm is made of a stack of Full-bridge SMs and a Director Switch (DS). These DSs are series-connected power transistors used to make the two arms of same phase leg conducting the AC alternately. The working principle of one leg is depicted on Fig.2. The voltage blocking capability of the DSs during the open state of an arm reduce the voltage requirement on the stack of SMs, hence reducing the total number of SMs in the AAC. The stack of SMs can provide the DC-Fault blocking capability if the maximum voltage generated by the SMs (Determined by the number of SM per arm) is enough to oppose to the AC grid voltages. In term of SM number, the AAC needs 34% less SMs than the MMC [7] for a full overlap period ($\theta_{ovl} = \pi/3$) and operating at the same DC bus voltage. Moreover, [9, 10] have shown that in addition to the decrease in the SM requirement, the stored energy requirement is lower than the MMC.

However, the AAC have some drawbacks. A former one was the 6-pulses rippled DC current, caused by the arms alternation, which required to be filtered with a bulky passive DC Filter designed in [9] and [11]. This problem has been fixed by using the Extended Overlap-AAC (EO-AAC) [12] with an Active DC filtering control strategy. Recently, [13] has proposed an active filtering stategy based on the energy control and proposes a novel Double-Overlap period to improve the filtering of the DC current however this technique increases the SM requirement. The second drawback is the lack of controllability of the AAC than the MMC when only one arm conducts. In this configuration, the conducting arm's current and the grid current are the same, leaving only one current to be controlled; thus limiting the control to either the power flow or the energy balancing of the converter. However, both controls are needed to ensure proper operation of the converter. If the grid currents control the power, the energy control can be achieved either by using the zero phase sequence third harmonic current injection discussed in [14] or by using the overlap current [15]. For both improved energy efficiency and safety reasons, the DSs should be zero-current soft switched, especially as they are in the direct conduction path of the arm and grid inductors. This issue is assessed in [16, 17].

In this work, an Overlap period is used to achieve the two aforementioned controls. During the Overlap period, both arms of one phase are operating simultaneously similarly to the MMC. This operating mode improves the overall controllability of the converter.

In summary, including Director Switches in the arm provides some very interesting properties to the AAC topology as mentioned above but also induces a more complex control with two main operating modes: Non-overlap and Overlap mode. In this latter, the energy and the DSs commutation controls have to be achieved requiring to split this mode in two parts. The Zero Current Switching method proposed in this paper is also a set of different sub sequences which have to be described accurately. Hence, to have a general and coherent overview of all this different sequences a sequential system representation tool is needed. The Petri Network may be a good solution, since it has been created to describe this kind of systems. All the sequences are associated to a place of the Petri Net where the actions realized in this place are described. The move from one place to another is characterized by a transition. Thanks to the use of the Petri net, a complete overview of this complex system is possible. Moreover, to each place is associated a model from which the control is deduced in a formal way thanks to the clear identification of the different key points of the AAC operations. This is also the originality of this paper to explain all the different types of model needed for the control design of all these places.

The paper is organised as follows. Section 2 presents the AAC main working principles in Non-overlap and Overlap modes and an identification of the control capability of each mode. Section 3 develops the Energy Control based on the AAC energetic model in overlap mode. In the section 4 is detailed a DS Zero Current Switching (ZCS) Control designed with technological and technical considerations. Finally, simulation results are given to support and validate the controls presented in the previous sections.

2. AAC Working Principles

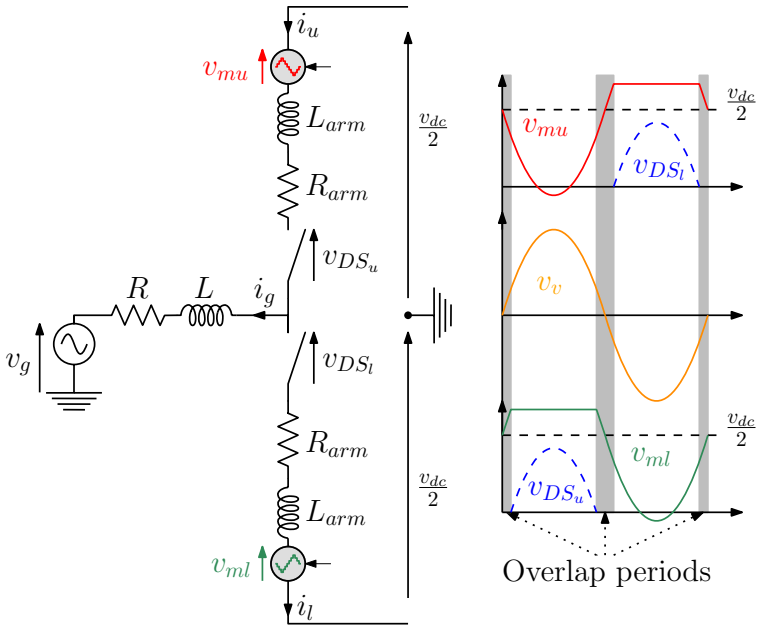

Figure 2: AAC Modulated and Director Switches voltages

As described by the AAC literature, switching from one arm to another (of the same phase) thanks to the DSs reduces the voltage constraint on the stacks of SMs, leading to reduced number of SMs per arm. However, they also introduce a discontinuous behaviour of the control that needs to be take into account for its design.

A first operating mode is identified, and called Non-overlap mode. In this mode, only one arm of each phase conducts the grid current and the other is opened thanks to its DS. During this operating mode, the converter suffers

of a lack of controllability as explained further. According to Fig.2 and by considering the lower arm of the phase 'j' opened it gives (for the upper arm):

$$v_{g_j} + (R + R_{arm})i_{g_j} + (L + L_{arm})\frac{di_{g_j}}{dt} = \frac{v_{dc}}{2} - v_{muj} \tag{1}$$

Considering the switching between the arms allows to deduce the switched current model in Non-overlap mode:

$$v_{vj} = G_{DSuj} \times (-v_{muj} + \frac{v_{dc}}{2}) + G_{DSlj} \times (v_{mlj} - \frac{v_{dc}}{2}) \tag{2}$$

With $G_{DS(u,l)j}$ the DS Gate signals and v_{vj} equals to:

$$v_{vj} = v_{gj} + (R + R_{arm})i_{gj} + (L + L_{arm})\frac{di_{gj}}{dt} \tag{3}$$

This model returned the AC voltage (v_{vj}) that need to be synthesized by the converter for a given PQ (Active and Reactive powers) set point. Then, it is distributed to the upper or lower arm according to the value of the respective gate signal. The main issue of this operating mode is the fact that only the grid currents can be controlled through v_v. Hence, if the grid currents control the power flow, the overall energetic equilibrium cannot be ensured and depends on an ideal operating point called Sweet-spot. This operating provide no energy deviation after one grid period. This operating point is obtained by equating the energies in the AC and DC side:

$$E_{ac} = E_{dc} \rightarrow \hat{V}_g = v_{dc}\frac{2}{\pi} \tag{4}$$

However, a voltage deviation of few percent can be observed in a transmission system, therefore the AC voltage cannot always respects the constraint expressed in (4). Hence, the overlap period has been proposed as a mean to provide the circulation of a current enabling the energy management.

2.1. Overlap Mode

The Overlap mode refers to an operating mode where the two DSs of one phase are closed at the same time and during a certain time called Overlap period. As presented in [6] the Overlap mode is activated when the grid voltage is about to cross zero to minimize the impact on the stacks of SMs rating. If the grid currents control the power, the Overlap mode has two main roles :

1 To maintain the energy stable.

2 To provide the opening of the DSs at zero current.

When both DSs of the same phase are closed, the AAC acts as the MMC and the two arms synthesize the AC voltage. So, with respect to the Fig.2 and considering no ON-state voltage drops across the DSs yields:

$$\begin{cases} v_{g_j} + Ri_{g_j} + L\dfrac{di_{g_j}}{dt} = \dfrac{v_{dc}}{2} - v_{muj} - L_{arm}\dfrac{di_{uj}}{dt} - R_{arm}i_{uj} \\ v_{g_j} + Ri_{g_j} + L\dfrac{di_{g_j}}{dt} = -\dfrac{v_{dc}}{2} + v_{mlj} + L_{arm}\dfrac{di_{lj}}{dt} + R_{arm}i_{lj} \end{cases} \tag{5}$$

In the same way as the MMC, a variable change is applied in order to control separately (as possible) the AC and DC side. These variables are given as follows:

$$i_{gj} = i_{uj} - i_{lj} \tag{6}$$

$$v_{vj} = \frac{-v_{muj} + v_{mlj}}{2} \tag{7}$$

$$i_{diffj} = \frac{i_{uj} + i_{lj}}{2} \tag{8}$$

$$v_{diffj} = \frac{v_{muj} + v_{mlj}}{2} \tag{9}$$

Thereby, it results a model where the AC and DC sides are decoupled:

$$\begin{cases} \left(R + \dfrac{R_{arm}}{2}\right) i_{gj} + \left(L + \dfrac{L_{arm}}{2}\right) \dfrac{di_{gj}}{dt} = v_{vj} - v_{gj} \\ R_{arm} i_{diffj} + L_{arm} \dfrac{di_{diffj}}{dt} = \dfrac{v_{dc}}{2} - v_{diffj} \end{cases} \tag{10}$$

Equations (10) reveal the possibility to control, during the Overlap period, the grid currents i_g thanks to v_v and the differential currents i_{diff} through the voltages v_{diff}. The active and reactive powers are controlled with i_g. Thus, the differential currents will be further used to achieve the energy management and the soft opening of the DSs.

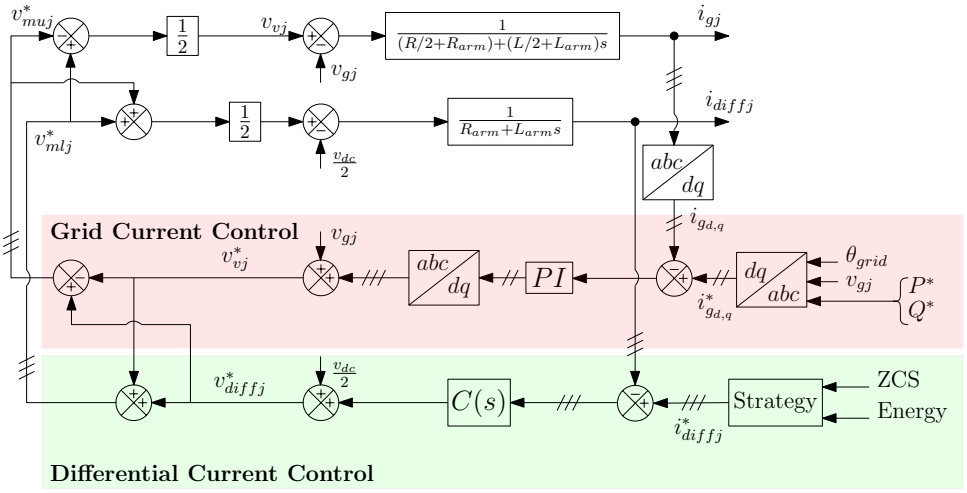

Figure 3: Current model and control of the AAC in Overlap mode

Fig.3 presents the two inner closed loops control implemented for the AAC. The variables noted 'x' are the measure while the others noted 'x^*' are the references. The control in the red frame is involved of the grid currents i_{gj}, they are controlled all along grid period, thereby, a classical PI (Proportional-Integral) controller in the dq frame is used.

Unlike the MMC, the differential current cannot be controlled out of the Overlap period. However, since there is always at least one non zero arm current, so, from a mathematical point of view, the differential current is not zero out of the Overlap period but only uncontrollable.

To control the differential current during this short period, different techniques have been explored such as the hysteresis controller [15, 18] which allows high dynamics in addition to a simple implementation. Recently, a current control has been proposed in [19] providing, among other features, a reduced switching frequency compared to the hysteresis controller. In this paper, a simple hysteresis controller is used, its principle is to activate positively or negatively one, or more, SM to vary the voltage across the arm inductors.

The Overlap mode provides a better control capability of the converter however it increases the arm conduction time leading to an increase of the SM number [7]. The number of SMs can be expressed thanks the expression (2), by introducing θ_{ovl} the overlap angle and the SM average nominal value V_{SM}:

$$N_{SM} = \frac{\hat{V}_{stack_j}}{V_{SM}} = \frac{\dfrac{v_{dc}}{2} - \hat{V}_{vj} \sin\left(\pi + \frac{\theta_{ovl}}{2}\right)}{V_{SM}} \tag{11}$$

With $\hat{V}_{stack_j}$ the peak positive voltage required to avoid distorsion on the AC voltage. To minimize the impact on the converter footprint and the losses, the Overlap period should be as short as possible (long enough to control the energy and achieve the DSs soft opening) to limit the SMs requirement. Mentioned in [18, 20], an adaptive control of the overlap length can be implemented accordingly to the energy deviation at the beginning of the Overlap period.

However, the converter is still designed for the worst cases (e.g. transients and large energy deviation), besides, in practical application it can be expected that the number of SMs is increased by ten percent similarly to the INELFE MMCs for redundancy and reliability purposes [21]. For this reason, this paper is not interested in the optimal design of the converter and considers instead a fixed value.

In the following, the grid currents reference i_g^* are defined by the PQ operating point. It remains now to determine the way to generate the references of the differential currents (i_{diff}^*). As it will be explained in sections 3 and 4, the converter internal energy as well as the DSs soft opening controls are achieved thanks to the differential currents. Therefore, these controllers give the references for the differential currents.

2.2. AAC Operating Modes Representation

Unlike the MMC which has continuous operations, the AAC is a sequential system following a repetitive set of different states. Therefore, graphical tools for the representation of sequential systems such as the Petri Network seem to be appropriate for this converter. By referring to Fig.4, this representation introduces places (P_x) representing the different AAC operations. To pass from a place to another, transition (T_x) must be validated.

During the Overlap period, the aforementioned controls must be achieved. The energy control is performed first and then the soft opening control of the DSs. Thereby, in each place corresponding to the Overlap mode (of one phase), sub Petri Networks are found to describe the sequencing during this mode.

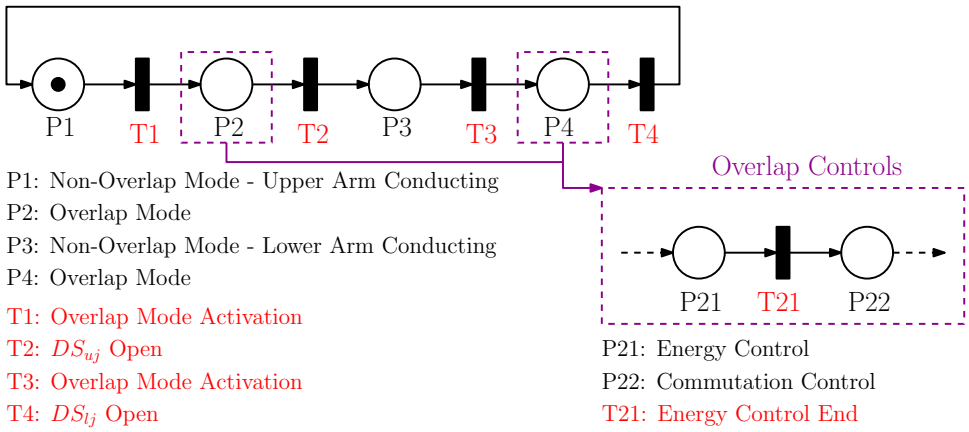

Figure 4: Petri Network of the AAC operations for the 'j' phase

Let us define:

- T_{ovl} : Overlap period
- T_W : Energy control duration
- T_{ZCS} : Soft opening control duration

The overlap period is defined as $T_{ovl} = T_W + T_{ZCS}$. In the next section, it is assumed that $T_{ZCS} << T_W$, thereby, the energy control is built around the assumption that $T_{ovl} \simeq T_W$.

3. Energy Control Design

The AAC is able to naturally stabilize its internal energy if the AC voltage respect the condition given by (4). However, operation at this specific ratio between AC and DC voltages is not feasible. Hence, the average values of the SM voltages may tend to deviate. Therefore, an active energy management to keep the SM voltages at their average nominal values is mandatory. For this study, an Average Arm Model is considered [22, 23], it replaces the stack of SMs by an equivalent chopper and an equivalent arm capacitor defined by $C_{tot} = C_{SM}/N_{SM}$ (See Fig.5).

To design energy controllers, another kind of model, called "energy models" are needed. The inputs of these models are the grid and differential currents references which are supposed to be equal to the grid and differential currents.

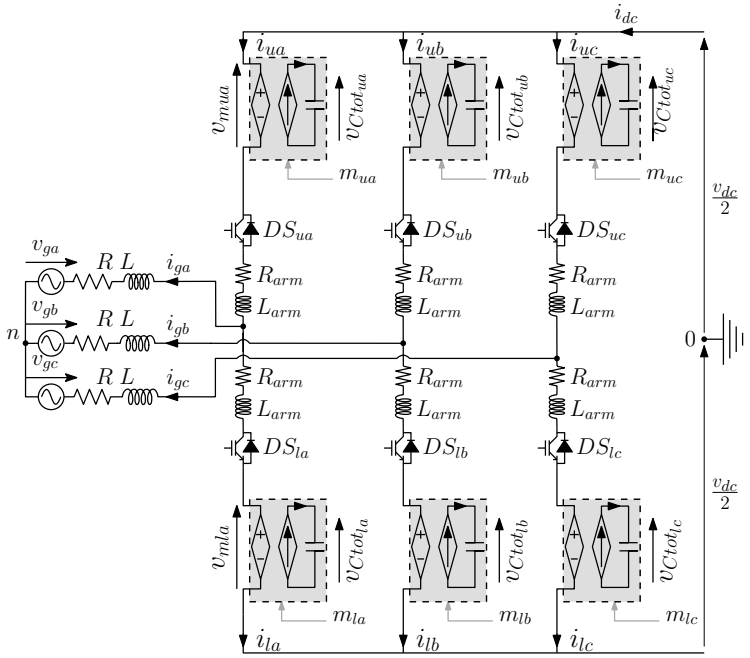

Figure 5: AAC scheme with Average Arm Model

3.1. Energetic Models

Based on Fig.5, the current flowing through the arm capacitor derived:

$$\begin{cases} C_{tot}\dfrac{dv_{Ctotu_j}}{dt} = i_{Ctotu_j} = m_{uj}\, i_{uj} \\ C_{tot}\dfrac{dv_{Ctotl_j}}{dt} = i_{Ctotl_j} = m_{lj}\, i_{lj} \end{cases} \tag{12}$$

The modulation indices are defined by using the Indirect Direct Modulation (IDM) as called by [19]:

$$\begin{cases} m_{uj} = \dfrac{v_{muj}}{v_{Ctotu_j}} = \dfrac{v_{diffj} - v_{vj}}{v_{Ctotu_j}} \\ m_{lj} = \dfrac{v_{mlj}}{v_{Ctotl_j}} = \dfrac{v_{diffj} + v_{vj}}{v_{Ctotl_j}} \end{cases} \tag{13}$$

Replacing the expressions of the modulation indices of (12) by those obtained with the IDM yields:

$$\begin{cases} C_{tot}\dfrac{dv_{Ctotu_j}}{dt} = \left(\dfrac{v_{diffj} - v_{vj}}{v_{Ctotu_j}}\right)\left(\dfrac{i_{gj}}{2} + i_{diffj}\right) \\ C_{tot}\dfrac{dv_{Ctotl_j}}{dt} = \left(\dfrac{v_{diffj} + v_{vj}}{v_{Ctotl_j}}\right)\left(\dfrac{-i_{gj}}{2} + i_{diffj}\right) \end{cases} \tag{14}$$

By multiplying respectively by v_{Ctotu_j} and v_{Ctotl_j} (15) is obtained:

$$\begin{cases} \dfrac{C_{tot}}{2}\dfrac{dv^2_{Ctotu_j}}{dt} = \left(v_{diffj} - v_{vj}\right)\left(\dfrac{i_{gj}}{2} + i_{diffj}\right) \\ \dfrac{C_{tot}}{2}\dfrac{dv^2_{Ctotl_j}}{dt} = \left(v_{diffj} + v_{vj}\right)\left(\dfrac{-i_{gj}}{2} + i_{diffj}\right) \end{cases} \tag{15}$$

By adding and subtracting the two expressions of (15) a set of simplified equations where appears the per-phase stored energy $\left(\frac{dW_j^{\Sigma}}{dt}\right)$ and the per-phase energy difference $\left(\frac{dW_j^{\Delta}}{dt}\right)$ is obtained. The equation (2) allows to show that in steady-state v_{diffj} is equal to the half of the DC bus voltage. Moreover, neglecting the voltage drops across passive elements gives $v_{vj} \simeq v_{gj}$. Thus, the following models are derived:

$$\begin{cases} \dfrac{dW_j^{\Sigma}}{dt} = v_{dc}\, i_{diffj} - v_{gj}\, i_{gj} \\ \dfrac{dW_j^{\Delta}}{dt} = \dfrac{v_{dc}}{2}\, i_{gj} - 2 v_{gj}\, i_{diffj} \end{cases} \tag{16}$$

Equations (16) present the instantaneous energy models. The energy deviation, from a physical point of view, can be seen as a difference between the power at the input and output of the converter after one fundamental cycle (grid period). Thereby, the control over the moving-average of the SM capacitor voltages is an acceptable solution. In this case losses are not considered, due to their negligible effect over only one cycle for a highly efficient power converters (>99%)[12]. To simplify notations, the single-phased power average value $\langle p_{acj} \rangle_T = P_{acj}$.

$$\begin{cases} \left\langle \dfrac{dW_j^{\Sigma}}{dt} \right\rangle_T = \left\langle v_{dc}\, i_{diffj}^{dc} \right\rangle_T - P_{acj} \\ \left\langle \dfrac{dW_j^{\Delta}}{dt} \right\rangle_T = \left\langle -2 v_{gj}\, i_{diffj}^{ac} \right\rangle_T \end{cases} \tag{17}$$

Knowing that v_{diffj} is a DC component and v_{vj} an AC one at the grid frequency, the differential current must be composed of a DC component $\left(i_{diffj}^{dc}\right)$ to control the average value of the stored energy and an AC component $\left(i_{diffj}^{ac}\right)$ to balance the energy between the upper and lower arms. These two expressions are the same as the MMC ones which could be expected since the AAC leg in Overlap mode is an equivalent MMC leg. Thereby, two energy controllers must be implemented, one for the stored energy and the other one for the energy balancing between the arms. However, the discontinuous behaviour of the AAC imposes to adapt these two generic models.

3.2. Stored Energy Control Design

Due to the AAC discontinuous operations, the energy is only controllable during the Overlap period. This specificity inherent to the AAC induces modifications on the basic stored energy model obtained in (17). Indeed, as explained in Section 2.1, even though i_{diffj} cannot be handled all along the grid current, this current, which is purely mathematical, is not null when the phase returns to its Non-overlap mode. That means that the term $\left(v_{dc} i_{diffj}^{dc}\right)$ is composed of two parts: A first one corresponding to the Non-overlap mode, not controllable, and therefore treated as a disturbance and the second one corresponding to the Overlap mode. This second part is the one that is possible to act on in order to adjust the average value of i_{diffj}^{dc}.

Hence, according the differential current waveform illustrated on Fig.6, the expression of the per-phase stored energy can be modified by taking into account the energy deviation during the Non-overlap mode.

$$\left\langle \frac{dW_j^{\Sigma}}{dt} \right\rangle_T = V_{dc} \frac{1}{2\pi} \int_0^{2\pi} i_{diffj}(\theta)\, \mathrm{d}\theta - P_{acj} \tag{18}$$

Assuming that during the Overlap period the differential current is equals to the DC component returned by the stored energy controller and during the Non-overlap mode equals to the half of the rectified grid current gives:

$$\left\langle \frac{dW_j^{\Sigma}}{dt} \right\rangle_T = V_{dc}\, i_{diffj}^{dc} \left(\frac{\theta_{ovl}}{\pi}\right) + V_{dc} \frac{\hat{i}_{gj}}{\pi} \cos\left(\frac{\theta_{ovl}}{2}\right) - P_{acj} \tag{19}$$

The model obtained in (19) integrates the energy deviation when the 'j' phase is in Non-overlap mode. This new disturbance is function of the instantaneous grid current peak value which means that this value must be updated

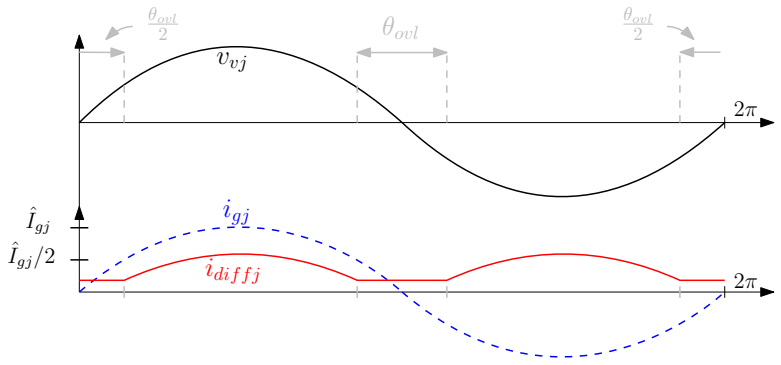

Figure 6: Differential current waveform

according to transient or event on the AC side. So, to simplify the implementation, it is proposed to express the disturbance induces by the Non-overlap with respect to the AC power.

$$\left\langle \frac{dW_j^{\Sigma}}{dt} \right\rangle_T = V_{dc}\, i_{diffj}^{dc} \left(\frac{\theta_{ovl}}{\pi} \right) + P_{acj} \left(\frac{2k_v^{acdc}}{\pi} \cos\left(\frac{\theta_{ovl}}{2} \right) - 1 \right) \tag{20}$$

With the k_v^{acdc} the ratio between the DC bus voltage and the peak AC phase to ground voltage (v_g).

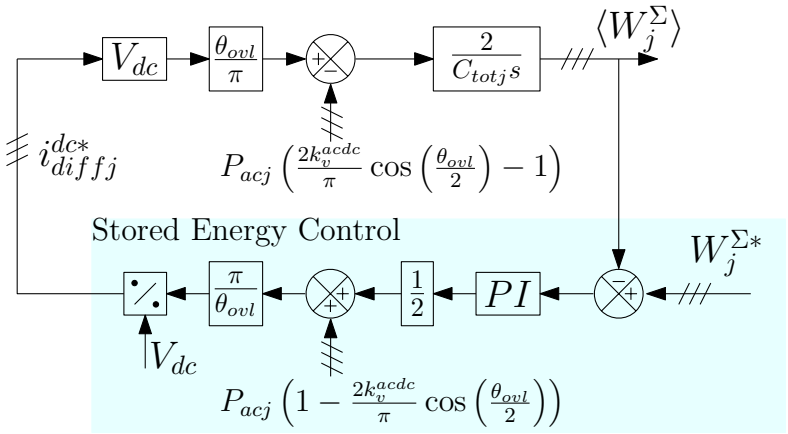

Figure 7: Model and Control of the AAC Leg stored energy

Fig.7 presents the model and control structure based on the direct inversion of this model. As described by the equation (19), the output of the stored energy controller is the instantaneous value of the differential current DC component that can be sent to the differential current control loop.

3.3. Energy Balancing Control Design

As presented in the section 3.1, an AC component is needed to keep the energy balanced between the upper and lower arms. The period of this AC component corresponds to the energy control time (T_W), so, the major part of the Overlap period. The energy balancing control is based on an algorithm which has for inputs: the grid angle, the voltages $v_{Ctot(u,l)j}$. The output of this algorithm is a square waveform with two possible angle values (0 or π)[24].

Fig.8 shows two cases (among four) where i_{diffj}^{ac} angle is chosen in order to charge or discharge the arm capacitors. This control computes if the slopes of v_{muj} and v_{mlj} are rising or falling (known thanks to grid angle) and the difference between the arm capacitor voltages.

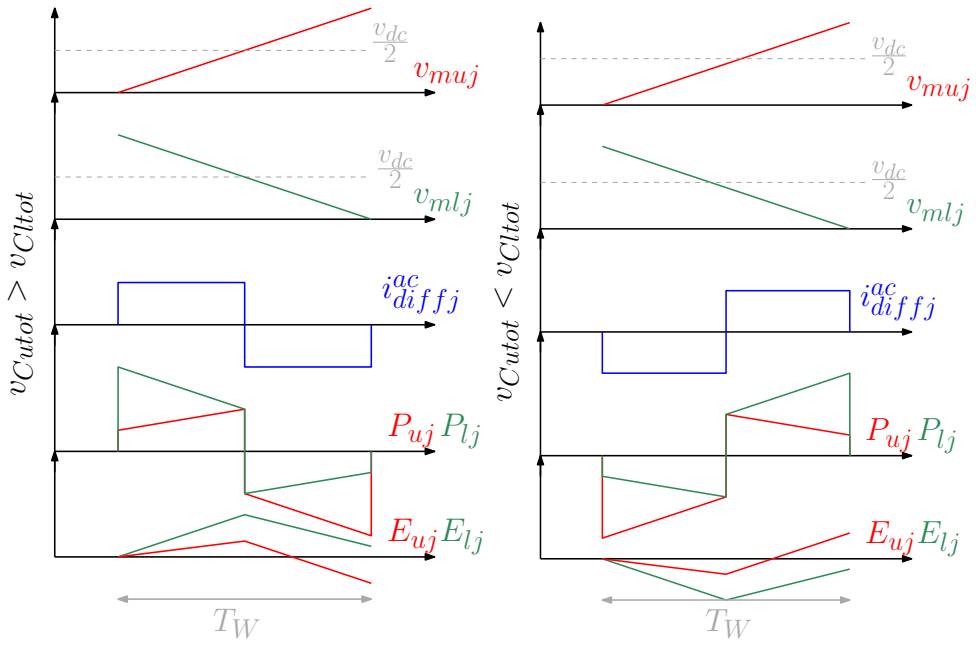

Figure 8: $i_{diff_{acj}}$ angle choice principle

Thanks to these parameters, the control can determines if the square waveform should be positive or negative first to balance the energy stored in the upper and lower arms. By taking into account the Overlap and Non-overlap modes, the energy balancing model is derived as follows:

$$\left\langle \frac{dW_j^{\Delta}}{dt} \right\rangle_T = -2v_{gj}\, i^{ac}_{diffj}\left(\frac{\theta_{ovl}}{\pi}\right) \tag{21}$$

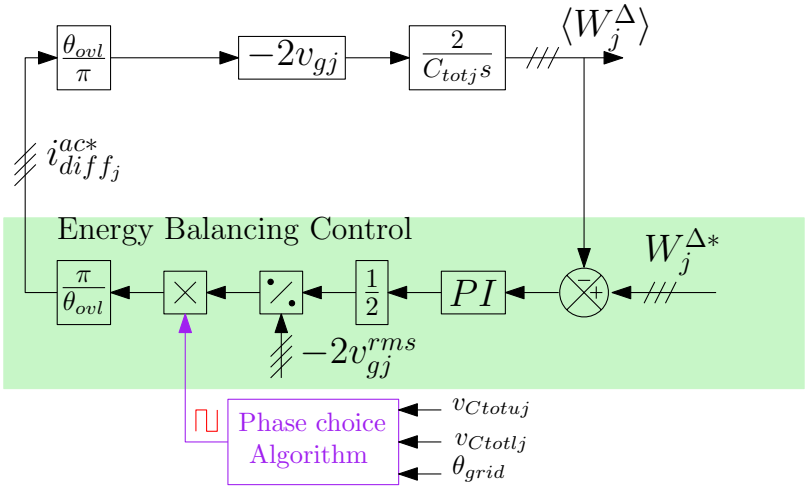

Figure 9: Balancing energy model and control

Fig.9 illustrates the model and the control structure of the energy balancing between the upper and lower arms.

This paper considers that the arms are perfectly symmetrical, i.e. their characteristics (e.g. impedance) are the same. In [25] this control is extended to operation under parameter variation.
The two parts of the energy controller (Stored and Balancing) generates two distinct differential current references which are added and sent to current controller.

4. Zero Current Switching Control Design

The time allocated to the DSs opening control (T_{ZCS}) should be as short as possible to maximize the energy control time (T_W) for a given Overlap period. The proposed method is designed and represented as a sequential process (Fig.10). This control considers that the DSs are composed of an association Transistor-Diode. Therefore, a Zero Current Switching means an opening of the DS with the diodes, since in this association, only the diodes switch naturally and softly at zero current. Hence, the proposed method aims to force the arm currents to flow through diodes allowing a soft switching of the transistors.

As mentioned above, this soft switching is possible with the control of the differential current. Indeed, as the MMC, during the overlap the arm currents are expressed as:

$$\begin{cases} i_{uj} = i_{diffj} + \dfrac{i_{gj}}{2} \\ i_{lj} = i_{diffj} - \dfrac{i_{gj}}{2} \end{cases} \tag{22}$$

These expressions show the possibility to control the arm currents either by the differential or the grid currents. However, it has be chosen to control the power flow with the grid current i_{gj}. Therefore, to cancel the arm currents, new references for the differential current must be calculated thanks to (22).

$$\begin{cases} i_{uj} = 0 \rightarrow i^*_{diffj} = -\dfrac{i_{gj}}{2} \\ i_{lj} = 0 \rightarrow i^*_{diffj} = \dfrac{i_{gj}}{2} \end{cases} \tag{23}$$

Nevertheless, using these references in practical cases will not ensure an opening at zero current. Indeed, some elements must be taken into account to propose a control allowing a soft opening in any case.

- The hysteresis band : Δi_{diff} (If an Hysteresis controller is used)
- The transistors turn-OFF time + ΔT_{OFF} (tolerance of each transistor) : T_{OFF}
- The measure precision (Sensor tolerance) : Δi_{sens}

These constraints allow to build a control which is tolerant against parameter variation in the power part. To take into account this three constraints ensuring a soft opening of the DSs, the coefficient Δi^*.

$$\begin{cases} i_{ui} = 0^{\pm} \rightarrow i^*_{diffi} = -\dfrac{i_{gi}}{2} + \Delta i^* \\ i_{li} = 0^{\pm} \rightarrow i^*_{diffi} = \dfrac{i_{gi}}{2} + \Delta i^* \end{cases} \tag{24}$$

The proposed method to open the DSs is designed with three sequences and illustrated with the Petri Net (Fig.10).

The following content considered the arm current cancellation for the upper arm current, a similar approach for the lower arm current is used. In all places, $i^*_{diffj} = -i_{gj}/2 \pm \Delta i^*$. The only modification is set on the value of Δi^*.

T21 $\theta = \frac{\theta_{ovl}}{2} - \theta_{zcs} + k\pi$: This transition is defined by duration of ZCS control.

P22-1 During this place, the arm current is forced to be negative with a low magnitude, just enough to make the diode conducting and avoid the arm current sign to change. Shown in purple on the Fig.11, Δi^* is negative and takes intro account the hysteresis band as well as the sensor accuracy.

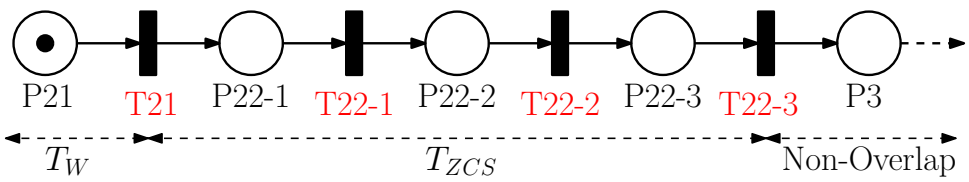

Figure 10: Petri Representation of the ZCS method

T22-1 $\left(\theta = \frac{\theta_{ovl}}{2} - \frac{2\theta_{zcs}}{3} + k\pi\right)$ & $\left(i_{diffj} == i^*_{diffj}\right)$: This condition is characterized by the time constant of the arm inductors and the dynamic imposed by the controller. To validate it, the arm current must be around it reference value during a certain duration.

P22-2 The differential current reference remains the same as in P22-1. At the beginning of this sequence, the DSs gate signals are modified and take the OFF state value. This place should be as long as the transistors need to be fully opened. Control margin has to be added since a commutation at zero current could takes more time for transistors than a hard switching.

T22-2 $\theta = \frac{\theta_{ovl}}{2} - \frac{\theta_{zcs}}{3} + k\pi$ This transition depends on the components turn off time with a margin. In the simulation results part, this time is fixed at 100μs corresponding to ten time steps.

P22-3 Once the transistors are all opened thanks to control margin added in P22-2, Δi^* is set positive to block the diodes when the arm current crosses zero.

T22-3 $\theta \geq \frac{\theta_{ovl}}{2} + k\pi$: It represents the end of the overlap period corresponding to a falling edge in the control.

Following the different places,the expected upper arm current waveform during the commutation control can be drawn (Fig.11) to illustrate the process. This waveform could be compared to the one obtained by simulation.

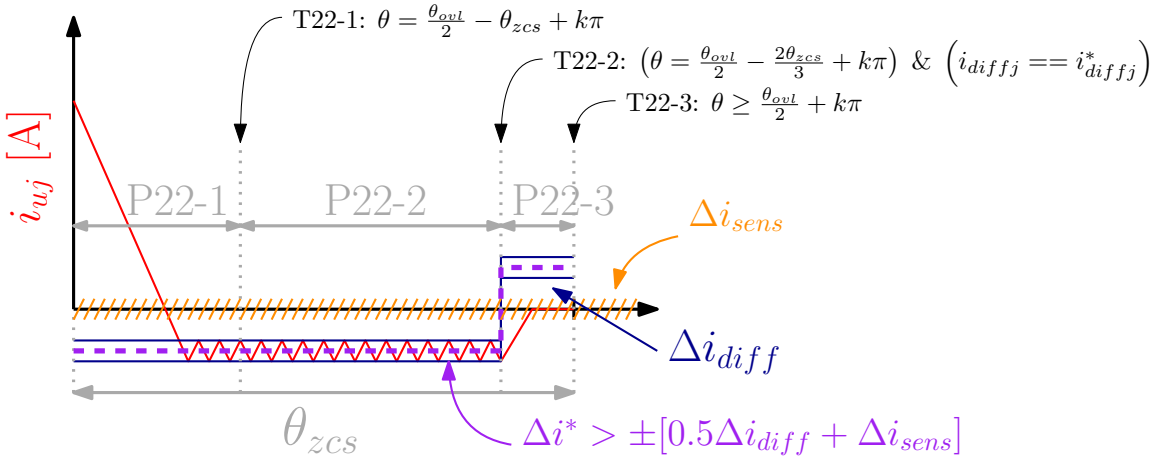

Figure 11: Theoretical arm current waveform during the ZCS control

5. Simulation Results

This section proposes to validate the different controls detailed in the paper. The simulation parameters are given in Table.1. The grid voltage have been chosen accordingly to the sweet-spot, and the DC bus voltage is the same as the INELFE link which is dependent of the cable technology. Different conditions are presented to validate the AAC controls. First, the energy control results are illustrated under 10% variation of the grid voltages with respect to the

sweet-spot (See (4)). Then, it is proposed to compare the upper arm current waveform obtained by simulation and the one shown in Fig.11 to validate the ZCS control of the DSs. All the results are presented for fixed Overlap angle ($\pi/6$) and ZCS control duration of 300μs. The hysteresis controller uses only one SM to generate the differential current.

To calculate the number of SMs required in each arm, (11) is used in addition to a margin of 10% as discussed in Section 2.1 . According to the parameters given above $N_{SM} = 293\,SMs$.

Parameters	**Values**
Active Power	± 1 GW
DC bus voltage	640 kV
AC grid voltage	407 kV ±10%
AC grid frequency	50 Hz
Phase inductance	60 mH
Arm inductance	1 mH
Overlap angle	$\pi/6$
Stack of cells rating	468 kV
Arm capacitor (C_{totj})	83 μF
Cell voltage (V_{SM})	1,6 kV

Table 1: Simulation Parameters

A first simulation is carried out to show the effectiveness of the energy control when a slope of 1GW/100ms is applied. To control the power with the grid currents, as discussed above, PI controller in the dq frame are used which is classical for VSCs. Fig.12 shows simulation results when a slope of active power is applied at t=0.05s. First it

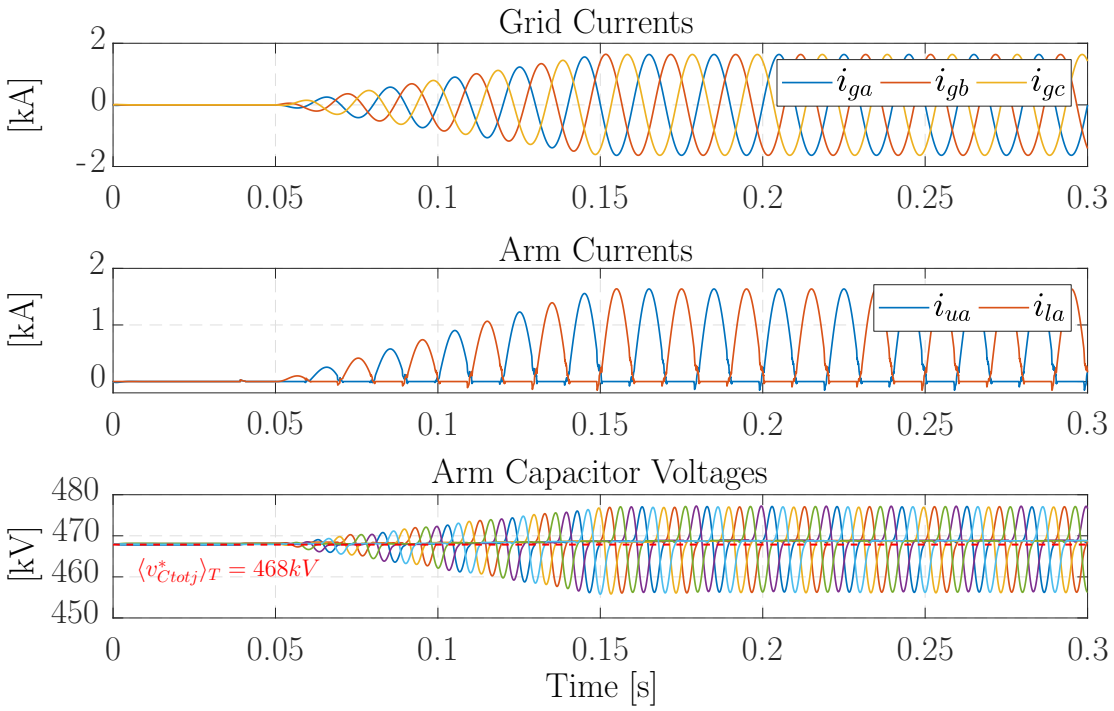

Figure 12: Energy Control test for 1GW transmitted power under sweet-spot condition

is visible that the grid current are well controlled and sinusoidal. Then, the second graph shows the arm currents of phase 'a'. In these currents two contributions are visible. In Non-overlap mode, only the grid current i_{ga} contributes to the arm currents. During the Overlap mode, the differential current i_{diffa} slightly modifies the waveform of $i_{(u,l)a}$ in addition to half of i_{ga}.

As shown in Table1 the sizing of the stack of cells (v_{Ctotj}) is done thanks to (11) and the sum of all the capacitor voltages gives 468kV with a margin of 10%. To be more competitive against the MMC, zero phase sequence voltage injection can be introduced in the control as discussed in [12, 26] to decrease the voltage constraint on the stacks. In red, dashed line, the references for each v_{Ctotj} is visible. The six arm capacitor voltages are shown, they are well balanced and centred around the nominal value of v_{Ctot}. When the power reference set point changes, all the controllers (Fig.7) try to reject the disturbance which is mitigated thanks to integration of the Non-overlap mode in the energy models. The stored energy controller response time (95% of the reference) has been fixed at 100 ms with a damping ratio of $\zeta = 0.7$. At t=0.3 s, the average value of each v_{Ctotj} is still at the nominal one . The previous simulation has tested the energy controllers under sweet-spot condition meaning a marginal energy deviation after one grid period. The next results proposes to results for larger energy deviation, thus, variation on the grid voltage of ±10% is applied.

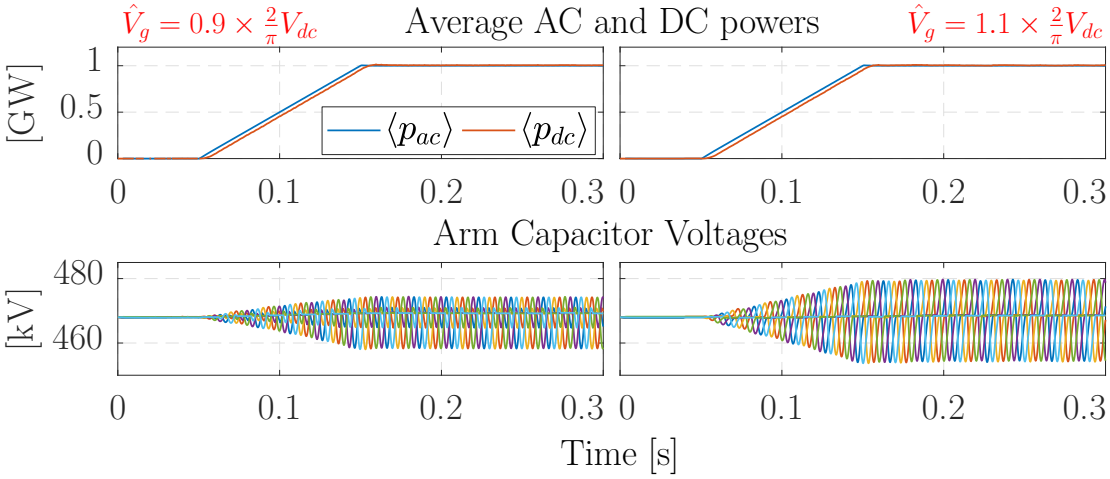

Figure 13: Energy control test under non Sweet-spot condition

The purpose of this second case is to show the efficiency of the control with operations under larger energy deviation, characterized here, by non Sweet-spot condition as illustrated on Fig.13. Similarly to the Fig.12, at t = 0.05 s a power ramp of 1GW is applied and it is visible that the energy is still well controlled even though the controller must returns a higher energy balancing current magnitude. In addition, Fig.13 depicts the average values of the AC and DC power to illustrate the energetic equilibrium in the converter obtained thanks to the energy controller meaning an equality between the input and output powers.

This papers has proposed the design of energy controllers based on the assumption that le low-level controller was perfectly (i.e. all the SM voltages are balanced). The next figure illustrates this controller by showing the voltage of the 293 SMs of the phase 'a' upper arm.

Fig.14 presents results of the low-level controller for each SMs. The average switching frequency in this example is 239 Hz using the hysteresis controller with a band of 50A. This frequency depends simultaneously of the high and low-level controller and the converter passive element design, thus a more complete study must be done to properly discuss about this aspect of the control.

The energy controllers have been validated under different conditions. It remains now to illustrate the ZCS control for the director switches. These results are shown on Fig.15.

The ZCS control simulation result is presented only for the upper arm current of phase 'a' (i_{ua}). This figure is focused only on the ZCS period (T_{ZCS}). The figure starts to plot curves near from the half of the overlap period, hence, a part of the energy control time is visible (0.27 to 0.2703). After this time, the control switch from the energy

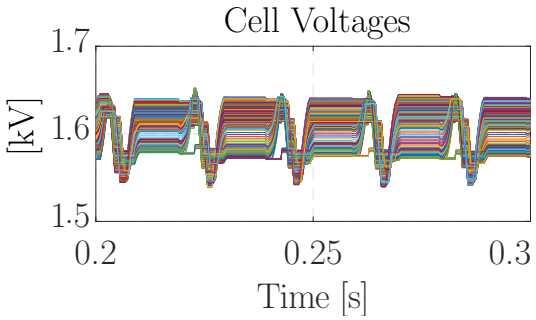

Figure 14: Low-level Controller validation

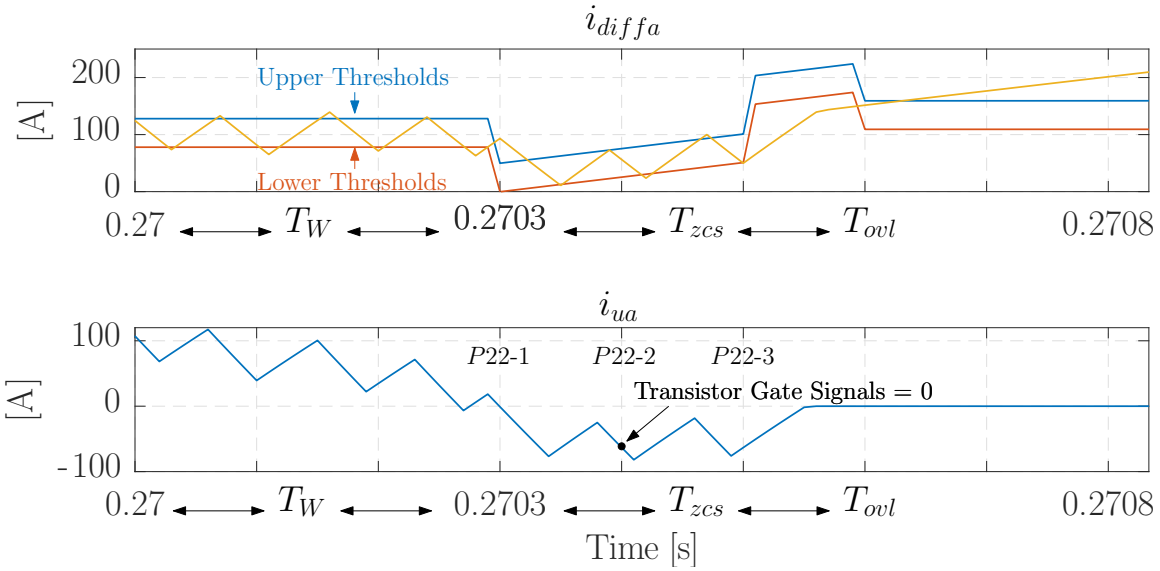

Figure 15: DSs commutation simulation results

differential current reference to the one for the arm current cancellation. It corresponds to the place P22-1 described in Fig.10. During this place, the arm current is forced to be negative and must compensate the hysteresis band to avoid zero crossing during the process. At the end of this place, P22-2 is activated and the differential current reference remains the same. The transistors are turned off and the arm current is maintained negative as long as the transistors need to be fully opened. Finally, in P22-3, the arm current is forced to be positive, however, since the transistors are opened the current is blocked at zero. At this moment, the voltage applied by the hysteresis controller makes the diodes reverse biased, hence they are naturally blocked.

6. Conclusion

This paper has discussed about the modelling and the control of an Alternate Arm Converter. Models in Overlap and Non-Overlap mode have been detailed and the converter control capability during each mode clearly shown. Using a step-by-step approach has allowed to describe the converter as a sequential system and the Petri Net representation has been used to illustrate the different AAC operations.

Including an Overlap mode in the control has provided a complete control of the internal AAC state variables. Based on the differential current control, an energy and a director switches commutation control were detailed.

The different controls proposed in this paper are supported by simulation. They have been tested under different conditions and have shown good performances. Investigation on advanced control techniques for the differential

current for decreasing the switching frequency during the overlap period would be interesting.

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