Multilayer CdHgTe-based infrared detector: 2D/3D microtomography, synchrotron emission and finite element modelling with stress distribution at room temperature and 100 K

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A B S T R A C T

The mechanical behaviour of a CdHgTe-based infrared detector was evaluated after processing at several temperatures to determine the impact of thermomechanical loading on residual stress and reliability. The architecture of the detector was first entirely characterized, relying on SEM, X-ray microtomography and diffraction analysis, in order to get the nature, the morphology and the crystallographic orientation of all the constitutive layers, and in particular the indium solder bumps. The results notably showed the unexpected single crystal aspect of the indium bumps with a repeatable truncated cone geometry. To obtain the thermomechanical response of the structure after processing and in the range of operating temperatures (from 430 K to 100 K), a 3D Finite Element model was then developed. As expected, the numerical results showed a stress gradient evolution in the structure from high to low temperatures, with high loca njvvl stress around 30 MPa in the CdHgTe at 100 K, mainly due to the thermal expansion coefficient mismatch between the different layers. They highlighted the significant influence of the geometry and the single crystal nature of the bumps as well as the behaviour law of the different materials.

1. Introduction

The demand to increase functionality and performance of electronic devices has led to the gradual miniaturization of electronic packaging. The flip chip process where the chip is assembled face down onto the circuit board is ideal for size considerations [1]: this architecture does not need extra contact area on the sides of the component and the connection length is minimised, which is relevant for high frequency applications. In the infrared detection field, the flip chip technology is exploited for several photodiode circuits in InSb, GaN, CdHgTe dedicated to different cutoff wavelengths. The packaging is complex and contains several materials such as metal, semi-conductor or underfill resin, which have very different mechanical behaviours (thermal expansion, elastic constants, among others). The interconnect size decreasing and the global architecture complexification lead to severe thermomechanical loadings during the manufacturing steps and running conditions: they can induce residual stress, mainly coming from the mismatch in the thermal expansion coefficient (CTE) of the various materials used [2], warpage or mechanical failure [3] in the microelectronic assemblies and affect their reliability. Such residual stresses have often been observed and quantified in thin or thick plates, for example after welding [4,5], with a great impact of tensile values on the structure integrity or fatigue limit, so that they should be rationalised. By approximating the structure to a thin film and the Stoney formulation [6] using the curvature of the substrate, it is possible to calculate the residual stresses in the chip above by neglecting the interconnection layer. This method is very limited and does not allow for an estimation of the evolution of stress through all the layers. Some experimental techniques such as Raman spectroscopy [7], X-ray diffraction [8] or Kossel Microdiffraction [9] can also be used, but they are limited in scope due to local heating, low electrical conduction or the thickness of the layers. The most common approach to estimate the stress values is to use Finite Element Method (FEM) and simulate the stack of chip and connections under thermal loading. If literature presents some papers about 2D representations [10,11], the increasing number of solder bumps in the assemblies led to the development of 3D models [12]. The results enable to observe a stress gradient throughout the architecture and in all directions. However, many hypotheses are often formulated concerning the material properties, with the different layers including single crystals usually assumed to be isotropic, and either plane stress or plane strain conditions are considered [13]. In the case of the interconnection zone, the shape of the solder bumps can be roughly assimilated to cylinders or truncated spheres while the material anisotropy is neglected, and to limit the number of elements in models, many authors propose to replace the interconnection layer with a homogeneously equivalent material [14]. These assumptions help to decrease the computing time and to model the whole assembly, but it makes it impossible to render

Layer	Crystallographic structure
CdHgTe circuit	Zinc blende
Silicon circuit	Diamond cubic
Indium solder bumps field	Tetragonal
Epoxy matrix	Amorphous

CdHgTe and solder bumps field thickness << silicon thickness

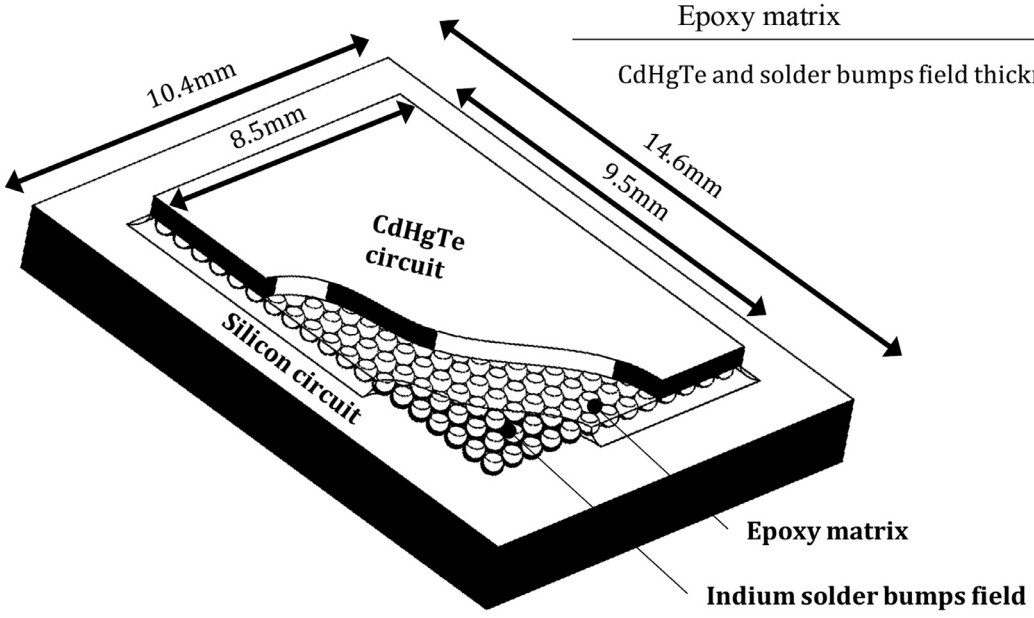

Fig. 1. Architecture of the IR detector considered.

a stress gradient in each layer [15] and they can lead to a misestimation of the stress values. Today, the main challenge for stress analysis in flip chip packages is the significant gradient at the micrometric scale. The interconnection layer can be very thin compared to the two interconnected circuits which can introduce high strain in the solder bumps. Moreover, the mechanical behaviour of the constitutive materials is often not well known. The modelling scale has to be adapted to the required observations and the impact of the input data on the results must be evaluated to determine what the most influential parameters are.

The present study aims at estimating the level of stress that appears in an infrared CdHgTe-based detector after processing at room temperature and at 100 K during service life. A 3D FEM model is developed to provide a better understanding of the strain/stress gradient in the structure under thermal loading and to improve the reliability. The relevance of such a model at a local scale strongly depends on the accurate knowledge of the actual architecture of the component. First, a characterisation step relying on SEM coupled to EDS and EBSD, X-ray microtomography and synchrotron emission has been carried out to apprehend the geometry, the chemical composition and the crystallography of all the layers of the structure, especially the indium solder bumps in the interconnection layer, which seems to be the most critical in the structure, considering the observed failure modes. From these considerations, a 3D FEM model was developed and thermal loadings representative of the component life cycle were applied. These simulations made it possible to show the stress gradients arising in the several layers at room temperature but also at operating temperature (77 K). A parametric study on the input parameters was then carried out to determine the most influential variables on the stress values. Finally, the stress distribution was compared to experimental values obtained at 77 K during a previous work using an X-ray diffraction method for single crystal.

2. Experimental procedure

2.1. Presentation of the detector architecture

This work considers a flip chip infrared detector (midwave-infrared MWIR) with a 30 µm pitch 320 × 256 I/O pixels IR focal plane array. The corresponding architecture is presented in Fig. 1:a CdHgTe thin layer (detector circuit) is interconnected to a silicon substrate (readout circuit) through indium bumps and an epoxy underfill.

This architecture leads to some symmetry with orthotropic properties: the indium solder bumps are aligned parallel/perpendicular to the edges of the detection circuit. Four main process steps are necessary to manufacture the detector (all steps are described in [16]): the indium bump depositing on the silicon circuit, the hybridisation of the CdHgTe detection circuit, the underfilling step and the final detection circuit thinning. During the hybridisation step, heating until 430 K is applied (above indium melting temperature); then both mechanical and chemical polishings of the detector circuit are performed to keep the active detection CdHgTe layer very thin compared to the thickness of the silicon circuit. During manufacturing and service life, the component is therefore subjected to intense temperature variations from 430 K to 77 K. The CTE mismatch between the CdHgTe detector chip, the interconnection layer and the silicon circuit is mainly responsible for residual stress initiation and warpage in the assembly that can lead to several failure modes such as solder bump damage or cracks in the CdHgTe chip. In order to better understand the appearance of residual stress, especially in the detection circuit and the solder bumps, the geometry and the materials constitutive of the different layers had to be precisely known to build the finite element model. A complete characterisation of the assembly was therefore carried out and particular emphasis was put on the interconnection layer and the solder bumps.

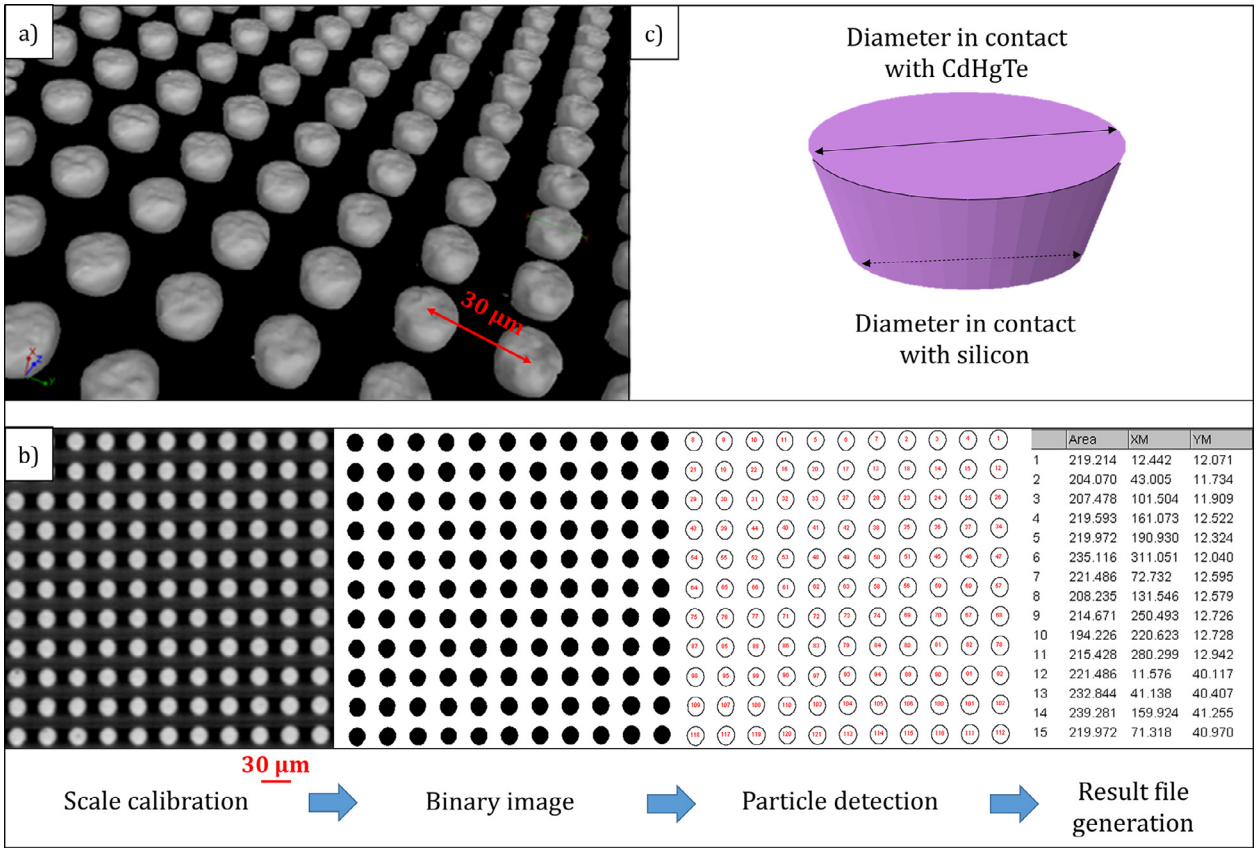

Fig. 2. (a) Solder bumps visualisation by microtomography (b) Example of a post-processing of the stack with ImageJ® (c) Solder bump represented as a truncated cone.

Table 1
Indium solder bump average thickness in both the centre and the edges of the component.

		Mean value	Standard deviation
Solder bump thickness (µm)	Component centre	6.52	6.54
	Component edge	0.11	0.13
Diameter in contact with CdHgTe (µm)	Component centre	17.4	0.16
	Component edge	16.8	0.19
Diameter in contact with silicon (µm)	Component centre	12.8	0.12
	Component edge	12.3	0.14

2.2. Geometrical characterisation

While the geometry of the silicon and CdHgTe circuits is well known, the morphology of the interconnection layer composed of solder bumps in an epoxy matrix still remains to be confirmed after the hybridisation step because visually inaccessible. In order to accurately model the structure, efforts have been made in X-ray microtomography to obtain the precise 3D description of the solder bumps in the centre and on the edges of the assembly. It has the advantage of being non-destructive, while achieving a very acceptable spatial resolution. This method exploits the selective absorption properties of the X-rays by the matter to observe the sample inside [17]: in a tomograph, the sample is illuminated with an X-ray source and the intensity modulations of the transmitted beam are recovered as an image by a 2D detector. During an acquisition cycle whose duration varies from a fraction of a second to several hours, some projections are collected according to different angular positions of the sample in rotation. The distance to the detector, the choice of the acquired image number as well as the angle step are realised according to the desired resolution. The reconstruction of 3D objects is made from the angular projections: a grey level is associated with each voxel of the volume, which informs on the attenuation coefficient of the matter. The analyses were realised using a Phoenix v|tome|x m 300/180 tomograph from General Electric Measurement and Control equipped with a 16 megapixel Dyn41-100 detector. The tube of the set up can reach an acceleration voltage of 180 kV and generate an X-ray beam allowing a very fine detail detection (down to 0.5 µm voxel size). Without any cutting, the analyses were performed with a 1 μm^3 resolution and led to a good estimation of the solder morphology and repartition. To be statistically representative, a large volume of the sample, approximatively $2.0 \times 2.0 \times 1.0\,mm^3$ was analysed, corresponding to a field of about 4500 solders bumps, both in the centre and at the edges of the component. After threshold application, the 3D visualisation of the solder bumps with the software MyVgl® was very precise, as shown in Fig. 2 (a).

The open source imageJ® software presented in [18] was used for part of the post-processing in the interconnection zone: an example is given in Fig. 2(b). By averaging solder diameters in all images, it was possible to visualize the typical geometry of an indium solder bump: the detailed dimensions are given in Table 1, with similar results in both the centre and the edges of the IR detector. The final 3D representation can be easily assimilated to a truncated cone (Fig. 2(c)), with maximum and minimum diameters in contact with the CdHgTe circuit and the silicon substrate, respectively.

Crystallographic orientation of the silicon single crystal

[uvw]	[011]
[u'v'w']	[0-11]
[hkl]	[100]

Crystallographic orientation of the CdHgTe single crystal

[uvw]	[1 -1 0]
[u'v'w']	[1 1 -2]
[hkl]	[1 1 1]

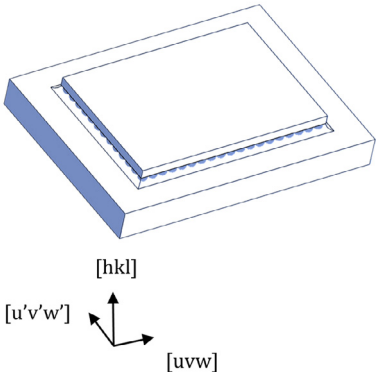

Fig. 3. Crystallographic orientation of the silicon and CdHgTe single crystals.

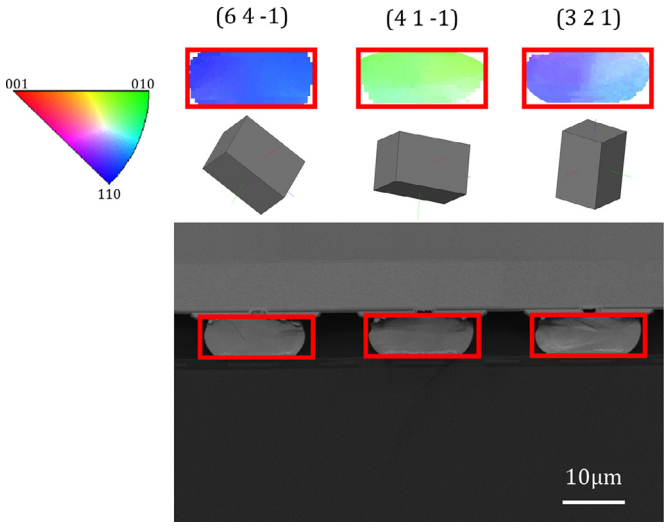

Fig. 4. EBSD mappings showing the mean crystallographic orientation of three indium solder bumps.

2.3. Crystallographic analyses

After the geometric characterisation of the indium solder bumps, it was necessary to determine the crystallographic nature of each crystalline layer of the structure in order to identify the relevant constitutive relation of each material to supply the finite element model. Electron Backscattered diffraction (EBSD) analyses were performed using a JEOL 7001F FEG SEM equipped with a CCD camera from Oxford Instruments. The CdHgTe and the silicon were easily accessible with the electron beam because they had emergent surfaces. The analyses established that they were two single crystals (111) and (100) oriented, respectively, as showed in Fig. 3, with a misorientation less than 1°.

Some components were cut and prepared with specific techniques in order to access the interconnection zone, especially the indium solder bumps. The sections were first carefully prepared (sawing and polishing) using a Leica EM TXP followed by ionic polishing with a Leica EM TIC3X. This last polishing technique provided ideal surface conditions for performing EBSD mappings with optimal indexing rate. The equipment used allowed ion cross-section cutting at room temperature or at low temperature when the setup was supplied with liquid nitrogen. Due to the low melting temperature of indium and its diffusion properties, the ionic polishing was carried out at 153 K with an acceleration voltage of 10 kV and performed in the centre of the assembly. Then, phase and orientation mappings were conducted on several solder bumps in the ionic polished area. EBSD mappings were performed with a beam energy of 20 kV, with a step size of roughly 0.5 μm; they were then post-processed using the Channel 5 suite. In total, a dozen indium solder bumps were mapped, showing that they were all single crystals with random orientation, as shown in Fig. 4. The EBSD orientation images are colour-coded to indicate the grain orientation given by the standard triangle (tetragonal lattice).

In order to confirm these observations considering a greater number of solder bumps, ring diffraction experiments were carried out on the beamline ID11 at the ESRF (European Synchrotron Radiation Facility) in Grenoble, France. As exploited by [19,20], this method allows to identify the several phases present in a sample. The measurements were performed with a 78.5 keV (λ=0.158 Å) monochromatic X-ray beam in transmission mode. A schematic representation of the experimental device is shown in Fig. 5(a). The 0.2×0.2 mm^2 incident beam corresponding to a field of about 40 indium solder bumps entered normally to the specimens, forming complete Debye–Scherrer rings from the several crystallographic phases of the structure. The 2D diffraction rings were recorded by a Frelon 2D CCD camera with a resolution of 2048×2048 pixels (47.2×47.2 μm^2 pixel size). A distance sample/camera of 288.2 mm was chosen to recover a maximum of diffraction rings while keeping an acceptable resolution for their proper indexing. The samples were placed in such a way that the beam was focused in the centre of the assembly, "full-chip" zone, to acquire the diffraction rings of the detection circuit, the interconnection zone and the reading circuit simultaneously. The idea was to penetrate first the silicon substrate with the X-ray beam and exit through the thinned detection circuit side to minimize the amount of material crossed by the diffracted beam coming from indium solders and limit the diffraction ring attenuation. An example of a generated diffraction pattern acquired by the camera is shown in Fig. 5(b).

The diffraction patterns obtained have both diffraction spots and complete rings. Each ring corresponds to diffracting planes {hkl} of a definite phase: it is composed of several individual spots diffracted at the same Bragg angle, each spot being generated by a grain in a diffraction position. It is therefore possible to identify the phases present in the assembly, their crystallographic structure as well as their polycrystalline or monocrystalline nature. Given the small beam size used, a complete ring will be characteristic of a polycrystalline phase with small grain size. In Fig. 5(b), the very intense spots correspond to silicon and CdHgTe single crystals; others are due to remaining phases. In order to index the diffraction rings and associate them to their respective phases, it is necessary to proceed to a preliminary step to determine their associated diffraction angles. The Fit2D software was used for post-processing to integrate the Debye–Scherrer rings and generate the equivalent of a 2θ scan [21]. The input data include the pixel size of the camera, the wavelength of the radiation considered as well as the camera-to-sample distance. These parameters are then refined; the user has the possibility to manually correct the centre of the beam and the non-orthogonality of the detector with respect to the incoming beam. This step can also be performed more accurately using a calibration material such as a nanocrystalline powder [22]. In our case, the calibration is based on diffraction peaks of the silicon, the less strained layer (because very thick compared to others). As shown in Fig. 6, several diffuse continuous diffraction lines/diffraction rings can be attributed to very thin polycrystalline layers in the assembly such as the Under Bump Metallization (UBM). The diffraction rings of indium have also been identified according to their diffraction angle θ associated to the {hkl} diffracting planes (surrounded lines/diffraction rings in the 2θ scan presented Fig. 6): they are discontinuous, showing the presence of only a few grains with different orientations.

This result confirms the conclusions from EBSD mappings on the cross sections analysed: each indium solder bump is a single crystal. This can be of crucial importance since the tetragonal crystal of indium leads to a highly anisotropic thermomechanical behaviour along the different crystallographic axes. The fact that it is present in a single crystal

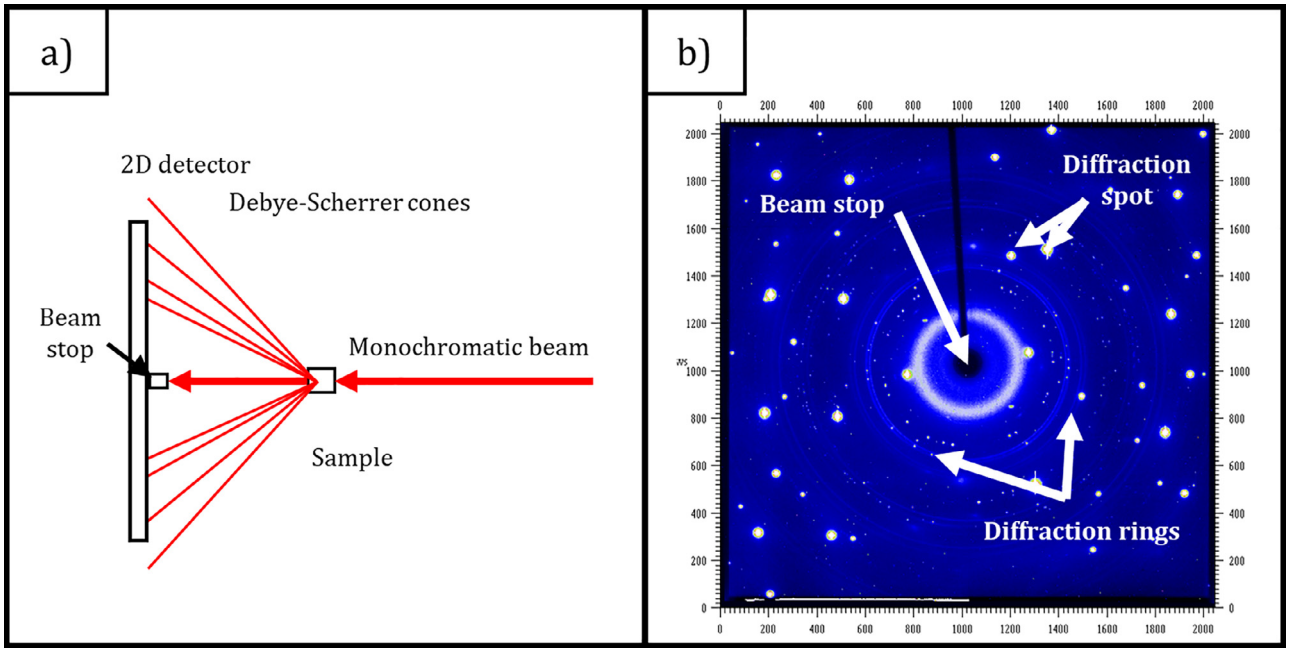

Fig. 5. (a) Diffraction ring set up (b) Diffraction pattern of the component acquired by the 2D detector.

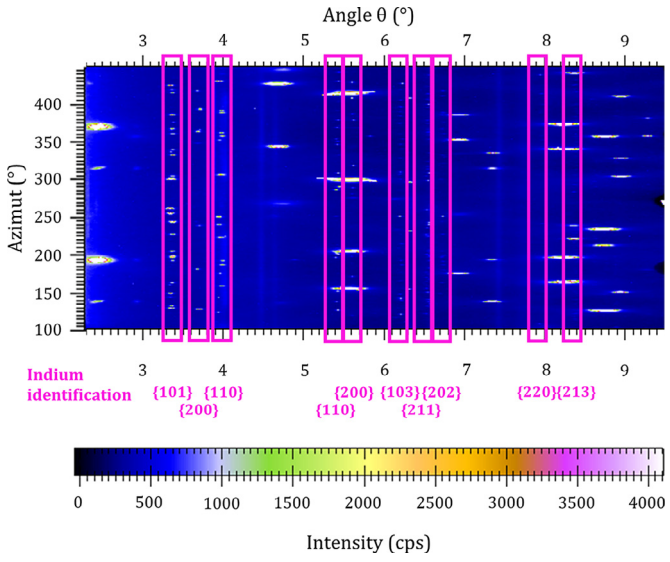

Fig. 6. Ring diffraction: identification of the discontinuous diffraction rings of indium.

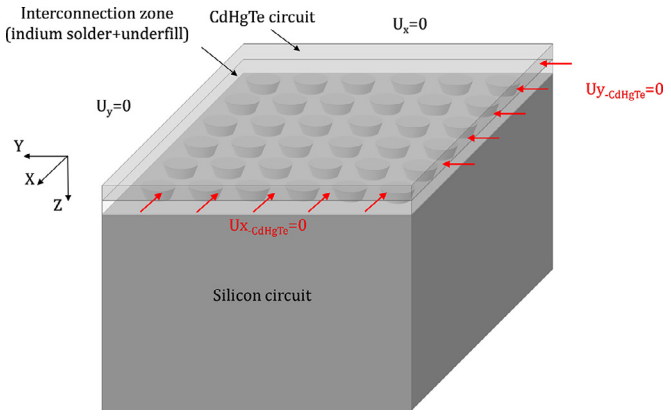

Fig. 7. Boundaries conditions considered for the 3D model.

form with random orientations in the IR detector can generate a mechanical response that can differ greatly from one indium solder bump to another (one pixel of the detector to another). Considering these various geometric and crystallographic observations, a 3D finite element modelling was built to simulate the complete stress distribution in the IR detector.

3. Finite element modelling

3.1. Architecture and meshing

The 3D FEM model developed in this work aims to show, at the scale of the layer or of a solder (that is a pixel of the IR detector), the presence of strain/stress gradients under thermal loadings and therefore to evaluate the impact of temperature variations on the stress level reached in CdHgTe, indium and silicon. It must be as representative of the actual geometry of the assembly as possible without necessarily modelling the entire structure, in order to highlight the effect of stress gradients on a very local scale by considering materials with very high heterogeneous properties. The underbumps metallization between the detection/readout circuits and indium solder was ignored in order to simplify the model and an ideal bonding along the material interfaces was assumed. Only the three main layers of the assembly were considered in the simulations:

- The detection circuit in CdHgTe.
- The interconnection zone consisting of a field of indium solder bumps embedded in an epoxy matrix.
- The silicon substrate.

The solder bumps were modelled as truncated cones as observed in the X-ray microtomography reconstructions.

The mesh of the CdHgTe layer and the interconnection zone (solders and epoxy matrix) was realised using linear hexahedral elements. At the interface with the interconnection zone, the first 50 µm of silicon were also finely meshed with linear hexahedral elements; then, a decreasing mesh was applied using quadratic tetrahedral elements in order to decrease the calculation time. This mesh allowed to obtain reliable stress

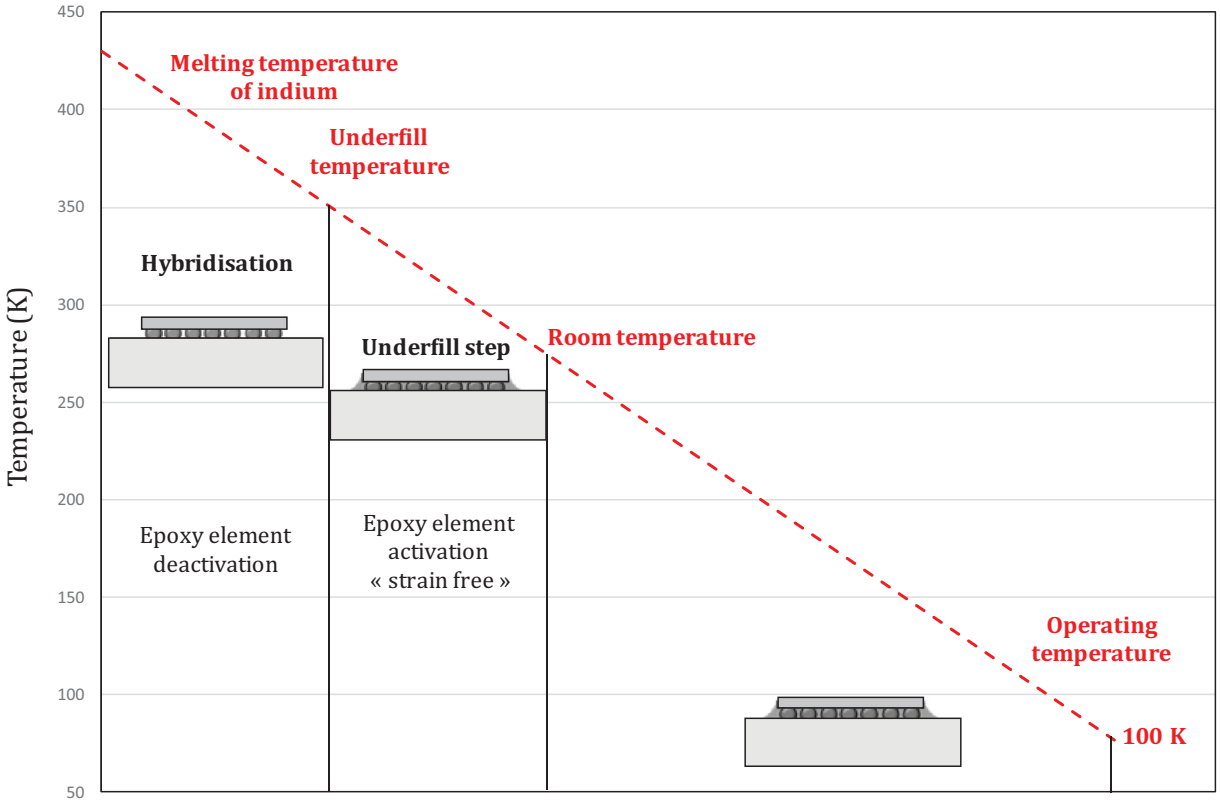

Fig. 8. Thermal loadings considered in the model.

distribution at the silicon surface: indeed, this layer is more than 40 times thicker than the combined detection circuit and interconnection layer, so that it is relevant to consider that it is only under loading at its extreme surface. A mesh convergence analysis showed that a size of 1.3 µm is necessary not to influence the stress values.

3.2. Geometric hypotheses, boundary conditions and thermal loadings

During hybridisation, before thinning, the detection circuit consists of two main layers, the CdHgTe epitaxial layer and a CdZnTe substrate [16]. In order to minimise the number of nodes in the model, the presence of the CdZnTe layer was not taken into account in the assembly. The thermal cycle is therefore applied to the geometry of the final detection circuit, so with only the active layer of CdHgTe. This is a required assumption to decrease the number of elements to mesh the silicon substrate, which is significantly thicker than the CdHgTe. The boundary conditions of the model are shown in Fig. 7. The structure has two planes of symmetry: conditions $Ux = 0$ and $Uy = 0$ respectively applied on two faces of the model (all the layers considered). Then, the underfill step induces the formation of an epoxy "beading" surrounding and rising on the flanks of the detection circuit: in order to take it into account (considering its thickness and the high difference of thermal expansion with the CdHgTe layer), the displacements of the latter were also limited ($Ux_{\text{-CdHgTe}} = 0$ and $Uy_{\text{-CdHgTe}} = 0$).

Although the thermal conductivity is different for all the constitutive materials, the assembly is assumed to have a homogeneous temperature at each computation time. The adopted thermal cycle is shown in Fig. 8. In order to simulate the underfill step, it was decided to deactivate the epoxy elements ("strain free") at the beginning of the calculation and to reactivate them at 353 K (Abaqus option), the glass transition temperature of epoxy, above which it was considered that epoxy didn't have any impact on the mechanical behaviour of the structure.

Table 2
Elastic constants of CdTe and HgTe.

	References	C_{11}	C_{12}	C_{44}	Uncertainty	Temperature (K)
CdTe	[25]	53.51	36.81	19.94	+/− 0.2%	298
	[26]	61.5	43.0	19.6	+/− 18%	77
	[24]	53.8	37.4	20.2	+/− 3%	298
		56.2	39.3	20.6	+/− 3%	77
HgTe	[27]	54.8	38.1	20.4	+/− 0.5%	290
		58.7	41.0	21.7		77
	[28]	53.61	36.60	21.23	+/− 0.8%	298
		58.63	40.59	22.41		78
	[29]	50.8	35.8	20.5		200

3.3. Material properties

The detection circuit consists of a (111)-oriented CdHgTe single crystal. While CdHgTe has high performance in the field of infrared detection due to its optical and electrical properties, it has much lower mechanical properties than other materials used for this application. It is generally considered as a "soft" material [23], with a very low mechanical strength. Due to the difficulty in measuring the elastic properties of a thin-film material, few data about the mechanical behaviour are available in literature: only values for the CdTe and HgTe manufactured with methods allowing to obtain large single crystals can be found. In this study, the stiffness tensors at room temperature and 77 K proposed by [24] for the CdTe have been used (Table 2).

The plastic behaviour of CdHgTe is also not well known. The yield stress has been estimated at 12 MPa by Ballet et al. [30]. This value can be impacted by a possible diffusion of the zinc present in the CdZnTe epitaxial substrate to the CdHgTe active layer before thinning. With 4% zinc in the CdHgTe [31], the yield stress can be multiplied by 4 for example, leading to a value of about 60 MPa; it has been fixed at 30 MPa in our model. The CTE proposed by Williams et al. [32] and Bagot et al.

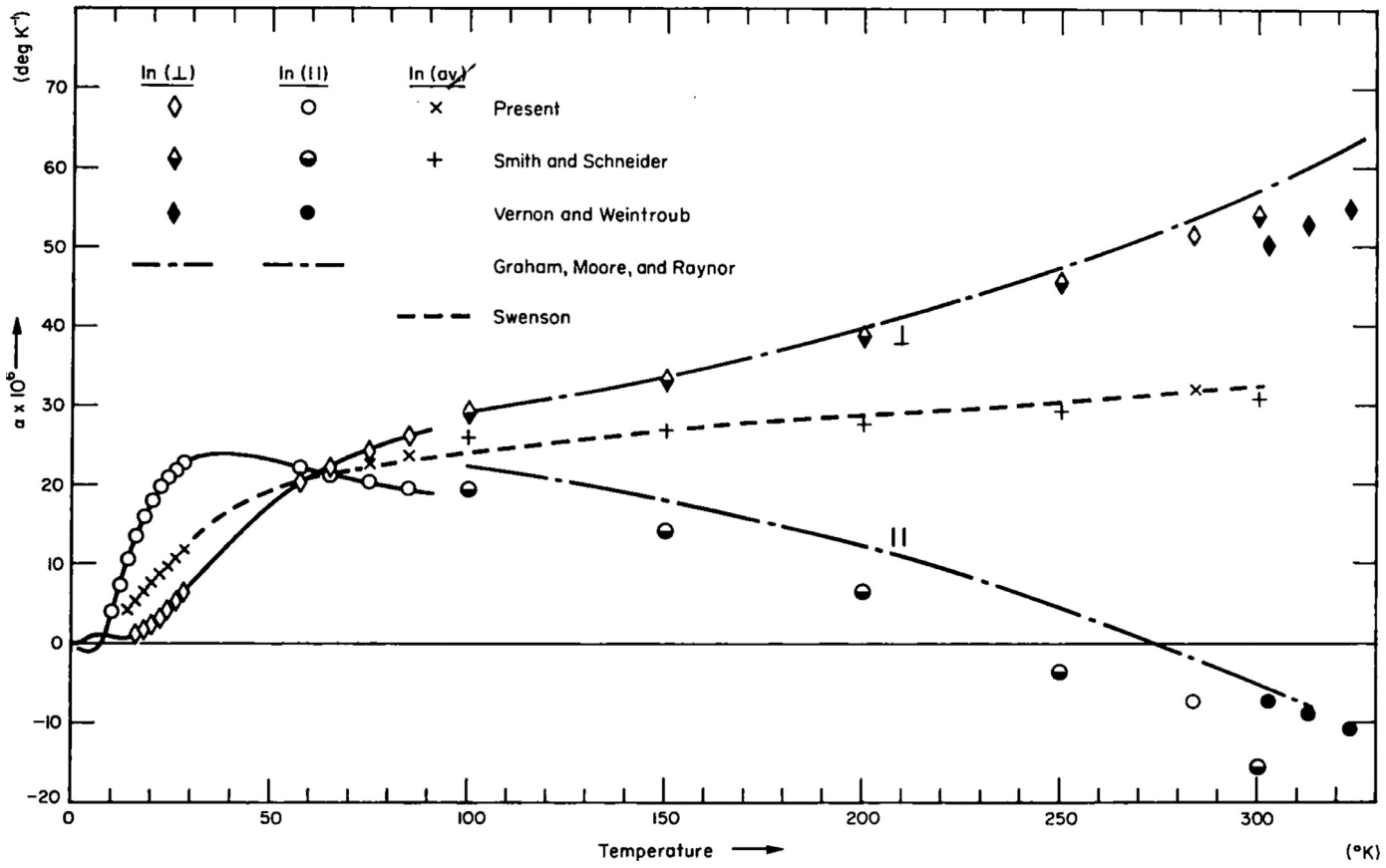

Fig. 9. Evolution of the CTE for indium single crystal as a function of temperature [36].

Table 3
Elastic constants of indium single crystal according to [37,38,39].

	[37]		[38]				[39]			
Elastic constants	300 K	77 K	298 K	300 K	351 K	371 K	391 K	412 K	422 K	429.7 K
C_{11}	45.35	52.6	445	45.1	43.3	425	42.1	41.4	41.1	40.9
C_{33}	45.15	50.8	444	45.3	43.5	42.9	42.3	41.7	41.3	41.1
C_{44}	6.51	7.6	6.55	6.53	6.3	6.17	6.03	5.89	5.83	5.78
C_{66}	12.07	16	12.2	11.9	10.7	10.3	9.88	9.46	9.21	9.05
C_{12}	40.01	40.6	39.5	39.7	39.8	39.6	39.5	39.1	39.2	39.1
C_{13}	41.51	44.6	40.5	41.1	40.9	40.4	40.3	40.1	39.9	39.5

[33] corresponding to a temperature range from 293 K to 693 K and from 0 K to 80 K respectively, have also been used. Indium is characterised by a low melting point, a small yield stress and a very high ductility at 293 K and 77 K. These properties combined with its high CTE compared to CdHgTe and silicon are very interesting for the interconnection layer when operating at low temperature. The mechanical properties of polycrystalline indium are well known: the behaviour laws from 4 K to 295 K have been determined by Reed et al. [34], confirming the high level of plasticity and the CTE given by Touloukian [35]. On the contrary, few data about indium under its single crystal form are available, but they point to a considerable anisotropy due to the tetragonal lattice with a notable ratio between the two lattice parameters c and a. For example, Collins et al. [36] showed that the CTE is very different along the axis of the crystal considered. Fig. 9 presents the results obtained for different authors, with In (‖), the CTE measured along the quadratic axis of indium, In (⊥), that measured according to a plane normal to the quadratic axis, and In (av), the average CTE.

The 6 elastic constants of indium for several temperatures were also determined by several authors (Table 3). Several simulations were then launched to compare the results considering the properties of indium as both polycrystal and single crystal.

Table 4
Mechanical properties of Epotek 301–2 as a function of temperature.

Temperature (K)	Young modulus (MPa)	Poisson's ratio
293	3664	0.358
250	4109	0.365
200	4474	0.349
150	5745	0.334
100	6993	0.350

Epoxy polymers (commonly known as epoxies) are widely used in microelectronics for the manufacture of flip chip assemblies to fill the interconnection zone between the chip and its substrate, that is to say to fill the gap between the solder bumps. The grade used in the IR detector is Epotek 301–2 and was characterised by Cease et al. [40] for temperatures ranging from 300 K to 100 K. The values of Young's modulus E and Poisson's ratio obtained are presented in Table 4.

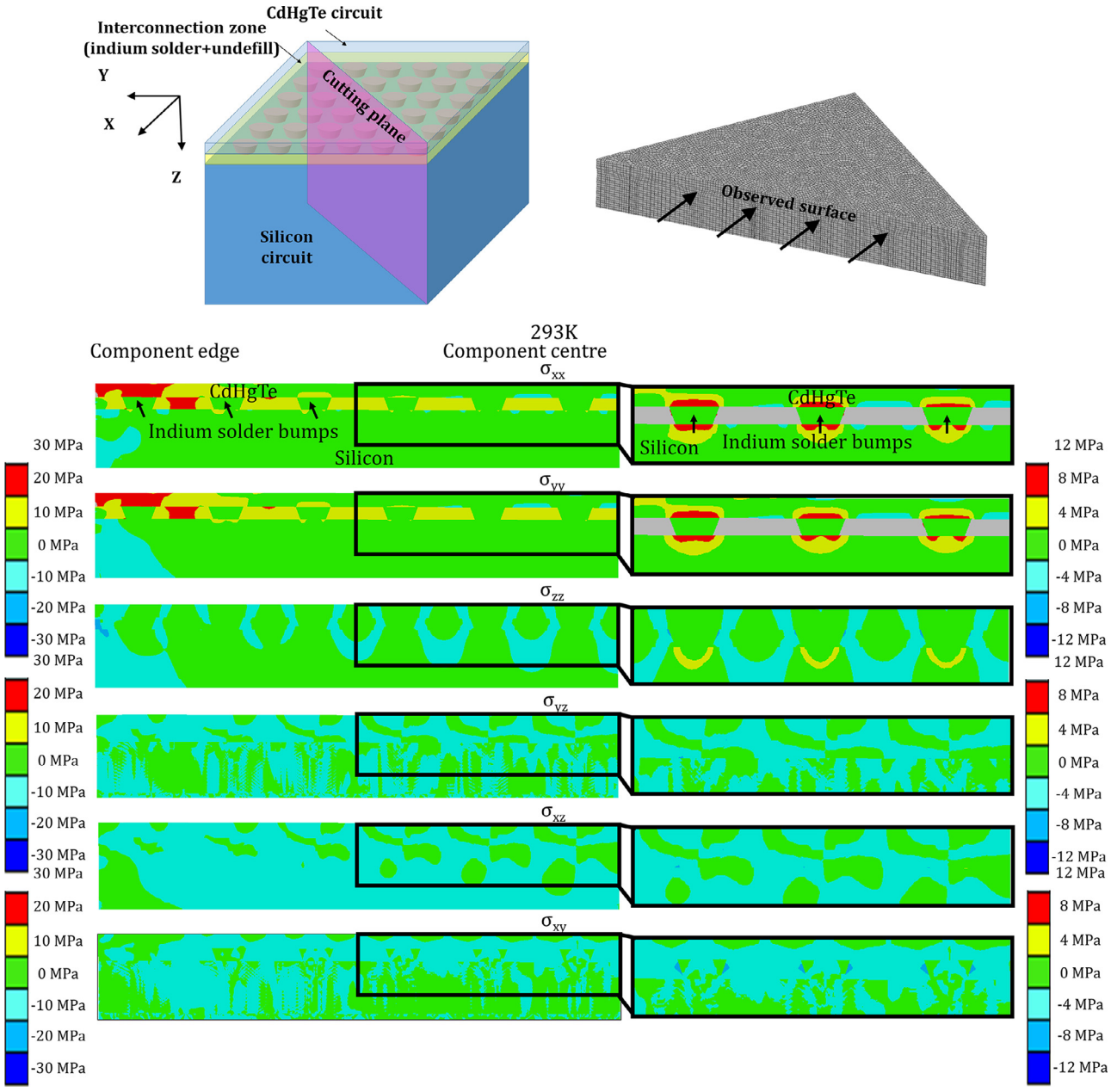

Fig. 10. Sectional view of the stress distribution in the different layers of the assembly at 293 K. The right part is a zoom of the framed zone with a finer scale.

At room temperature, Epotek 301–2 has a purely elastic behaviour with a yield stress/strength around 40 MPa. It will then vary significantly with temperature, as most of thermoplastics, with a glass transition temperature Tg=213 K; the manufacturer indicates that the CTE is 61.10^{-6} K^{-1} below this temperature and 180.10^{-6} K^{-1} beyond it.

The substrate of the component is an oriented silicon single crystal (100), the behaviour of which is elastic, with a yield stress/strength close to 130 MPa. The C_{ijkl} elasticity constants considered for the model came from [41] and the CTE as a function of temperature from [42].

For all the single crystal materials, the elastic constants are implemented in the Finite Element model in a two-step-process. First, basing on the experimental results, the crystallographic orientation of CdHgTe, silicon and the indium bumps are identified and the elastic constants are given in the crystal basis for each material. Then, the orientation of each crystal is introduced in the Finite Element model (where a global coordinate system imposes the global orientation) through a specific calculation that acts as a transfer matrix between each crystal and the global coordinate system.

4. Results and discussion

4.1. Simulations with polycrystalline indium solder bumps

The 3D modelling strategy allows to visualize the stress gradients along the thickness, in all the layers of the assembly, through a well-defined cutting plane. The main drawback of the FEM simulations is the computational time. To see the strain/stress gradient at the solder scale, it is not possible to model the totality of the structure (more than 80,000 solder bumps). First simulations with 36, 144, 324 and 1296 solder bumps were launched and showed that 144 were representative of the whole assembly, with converging results. In this paper, all the representations of the stress variation appearing in the assembly were visualized using diagonal sections. Only half of the architecture is presented in the following figures showing the edge and the centre of the structure due to the symmetry conditions. At 293 K, we notice that in the CdHgTe layer, the components of the stress tensor taking the highest values are σ_{xx} and σ_{yy}, close to 30 MPa the edges and

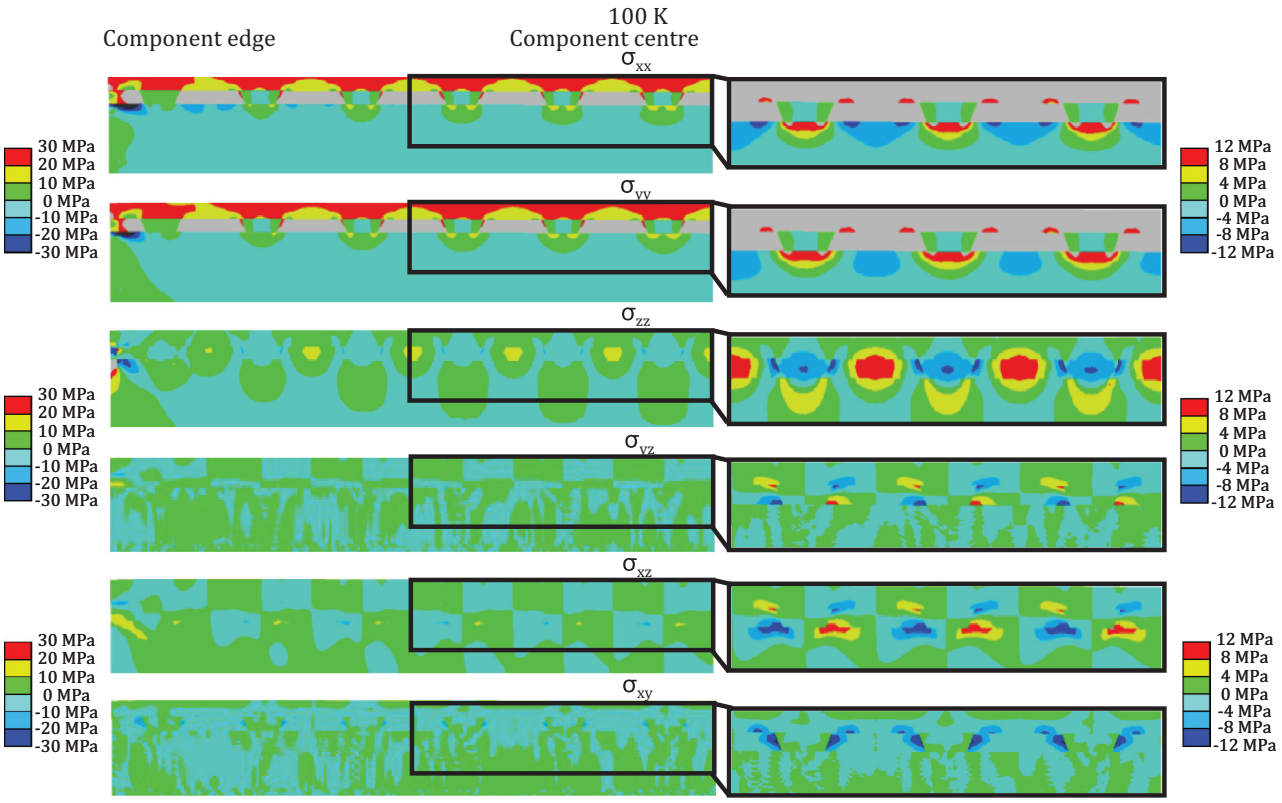

Fig. 11. Sectional view of the stress distribution in the different layers of the assembly at 100 K. The right part is a zoom of the framed zone with a finest scale.

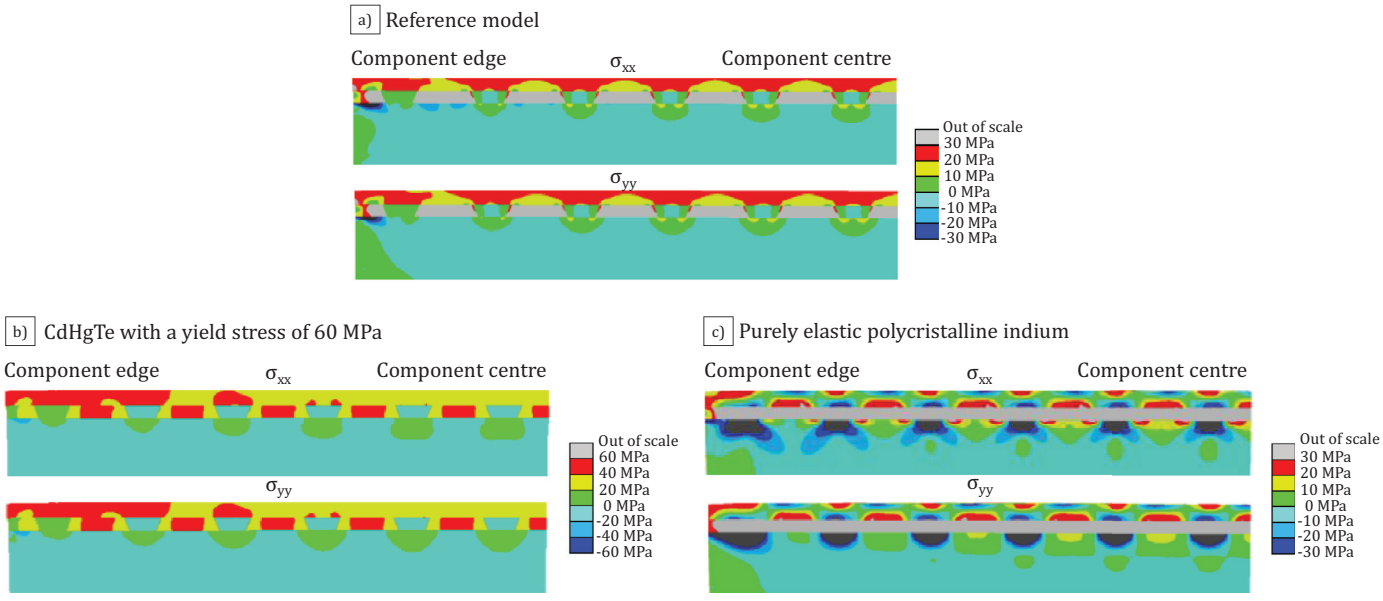

Fig. 12. Comparison of the numerical results (a) Standard model (reference) (b) CdHgTe with a yield stress of 60 MPa (c) Polycrystalline indium with a purely elastic behaviour.

around 10 MPa in the centre (Fig. 10); a zoom on certain zones makes it possible to highlight greater tensile values in the areas in contact with the solder bumps. The epoxy is in uniform biaxial tension around 15 MPa and the indium solder bumps are also in slight tension for σ_{xx} and σ_{yy} (2 MPa); the silicon is in biaxial tension with values ranging from 4 MPa to 12 MPa under the indium solder bumps. Finally, it can be noted that the affected silicon depth under the solder is approximately 8 µm.

When cooling at 100 K, interesting results can be noted (Fig. 11):

- Biaxial tension is intensified along σ_{xx} and σ_{yy} in the CdHgTe, with values from 30 MPa above the solder bumps to 18 MPa in the inter-solder areas; the epoxy shows some values outside the scale presented (grey area: 35 MPa on average for σ_{xx} and σ_{yy}). This is consistent with the experimental stress values obtained in [43], in which the authors used X-Ray Diffraction (XRD) with a 0.8 mm^2 beam to make some mappings from the centre to the edge of the CdHgTe chip: in particular, the measurements at 77 K showed tension stress values up to about 30 MPa.

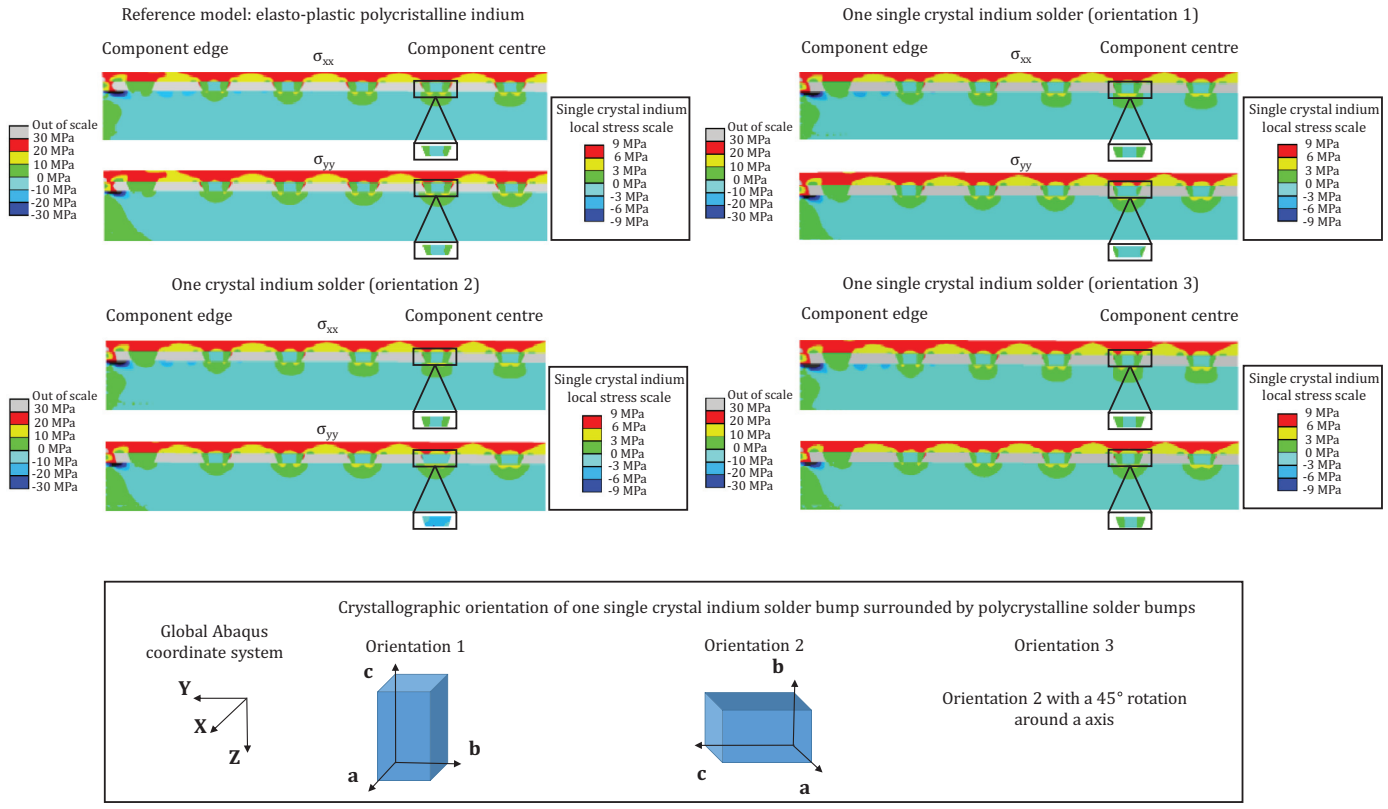

Fig. 13. Influence of one indium solder bump modelled as single crystal: different crystallographic orientations and thermal expansion coefficients considered (100 K).

- The solder bumps at the edge of the assembly are in tension, while those in the centre are in compression with tension in their periphery (for both σ_{xx} and σ_{yy}). This particular stress state is related to the difference in the CTE between the epoxy matrix and indium (61.10^{-6} K^{-1} and 30.10^{-6} K^{-1}, respectively).
- The stress variations in the silicon are enhanced with the apparition of compression values of about −7 MPa according to σ_{xx} and σ_{yy} in the zones under the epoxy.
- The layer with the most important values in σ_{zz} is the interconnection zone, with solder bumps in compression and the epoxy in tension.
- The values of σ_{yz} and σ_{xz} are amplified, especially in the CdHgTe and the silicon between the solder bumps. The epoxy is also slightly affected.
- Finally, the values of σ_{xy} are generally low: only the epoxy locally reaches compression levels around −12 MPa in the areas in contact with the indium solder bumps.

The results show the great influence of the mechanical properties and the CTE mismatch between each layer of the structure on the stress values. The stress gradients can be appreciated at two scales: between the edge and the centre of the assembly, and at the local scale considering one solder bump/pixel of the IR detector. The difference between the edge and the centre is typically due to the CTE mismatch between the CdHgTe and the silicon. Indeed, the CdHgTe detection circuit can be assimilated to a thin film compared to the silicon circuit thickness. The CdHgTe has a CTE twice smaller than the silicon, which explains the induced tensile stress state appearing during cooling from 430 K to 100 K. The stress gradient is higher at 293 K than at 100 K because the CdHgTe has started to yield, so that the biaxial tensile state of CdHgTe tends to be uniform at low temperature (around 30 MPa according to σ_{xx} and σ_{yy}). To keep the static equilibrium of the structure under the increasing tensile state of the CdHgTe layer, a low compressive mean state appears in the silicon substrate. Moreover, stress heterogeneities in the solder zone appear at 293 K and are enhanced at 100 K: this phenomenon corresponds to the mismatch between the CTE of CdHgTe, indium, epoxy and silicon. The silicon is in compression under the epoxy (−10 MPa to −20 MPa) and in tension under the solders (8–18 MPa) within a depth of a few microns. Thus, using a polycrystalline behaviour law for indium, heterogeneities can already be observed under thermal loading, whether it is pixel by pixel or between the centre and the edge of the detector.

4.2. *Influence of the input parameters*

In this section, the focus is made on the influence of the input parameters of the model on the numerical results. As explained in 2.4, one of the sources of uncertainties to predict the stress distribution in the IR detector is the lack of knowledge about the CdHgTe thermomechanical properties. Several simulations considering the different elastic constants proposed by all the authors (Table 3) have shown a very low impact on the stress values in all the layers at 100 K (<1%). The question of the plasticity of the CdHgTe is also very important, especially due to the possible diffusion of Zn coming from the CdZnTe substrate before thinning. In the results presented in Section 3.1 (Fig. 12(a)), the yield stress of the CdHgTe was fixed at 30 MPa, a value estimated from literature and the residual stress measurements presented in [43]. Other simulations with a yield stress of 60 MPa were launched (Fig. 12(b)) and showed the great impact on the numerical results since the maximal stress values observed were of the same order of magnitude. A stronger stress gradient was also observed in the CdHgTe layer between the edge and the centre of the assembly. On the contrary, neither silicon nor indium was really affected, due to their thickness and their high plasticity, respectively. It is therefore very important to well define the mechanical behaviour of the CdHgTe in order to get stress values as representative as possible with the model. In the flip chip FEM field, most

of the authors made the hypothesis that circuit and solder materials could be considered as purely elastic [11,14]. The material properties of indium announced by Plötner et al. [44] showed a very low yield stress with high plasticity. A pure elastic law for indium was also implemented in the model for comparison (Fig. 12(c)). The values of σ_{xx} and σ_{yy} in this case were thus very different: the silicon below the indium solders was more stressed with negative values out of the represented scale (−30 MPa), while the CdHgTe just above was in compression contrary to the previous results. As for indium, it was in high tension with stress values out of scale. These results were the direct consequence of the absence of plasticity in indium: the stress values increased without any limitation.

4.3. Influence of crystallographic orientation for indium solder bumps as single crystals

Since the EBSD and XRD results showed that each indium solder bump was a single crystal, complementary simulations were launched considering this particular aspect. More specifically, the aim was to see if the great anisotropy of the crystallographic orientation and the CTE of indium presented by Collins et al. [36] could increase the stress gradients in the assembly, especially at low temperature, since the solder expansion/contraction under thermal loading was supposed to affect the level of stress in the other layers. Several simulations were launched considering only one indium solder bump as a single crystal and the others as polycrystalline. Fig. 13 presents the results obtained for three different orientations of one solder bump at 100 K, in particular those for which the difference is maximised (anisotropy enhanced for mechanical properties and CTE), when considering the different axes of the tetragonal lattice of indium. They show a weak impact on the stress distribution in the CdHgTe just above, and if the indium solder bumps are mostly in tension with low compression in the centre at 293 K and 100 K, when polycrystalline or single crystals with orientation 1 or 3, some of them can be fully in compression with higher stress values due to their crystallographic orientation and the particular evolution of the CTE (especially for orientation 2). It should noted that this effect is similar when considering all the solder bumps as single crystals, with orientations close to orientation 2 always inducing higher stress/deformation in the bump. These local variations in the stress values can lead to possible solder cracks at the interface with the CdHgTe and/or silicon layers and explain the “randomly supposed” apparition of defects such as dead pixels in the detector.

5. Conclusions

In this work, the strain/stress evolution in an IR detector subjected to thermal loadings during its cycle life has been numerically studied. Conclusions of this study can be summed up as follows:

- The experimental results gave a very detailed description of the detector structure. The tomography analyses led to an excellent definition of the 3D solder bump geometry after the last process step. EBSD and ring diffraction provided a first two-dimensional description of the nature and crystallography of the different layers. The most important points are the presence of CdHgTe and silicon single crystals as well as the single crystal nature of indium solders and the random repartition of their crystallographic orientation, a feature that until now was completely unknown. They could subsequently be implemented in the finite element model with their anisotropic mechanical properties, which was essential for the model development to simulate strain/stress heterogeneities at the scale of one pixel of the detector.
- The finite element model was very useful to observe local heterogeneities inside the CdHgTe and silicon layers and to estimate the stress level in each indium solder bump. Heterogeneities appeared at the scale of the solder bump at 293 K and were amplified at 100 K. Whereas the biaxial tensile state of CdHgTe tended to be uniform at low temperature (around 30 MPa according to σ_{xx} and σ_{yy} consistent with the values obtained experimentally at 77 K [43]), silicon was in compression under epoxy (−10 a −20 MPa) and in tension under the solder bumps (8–18 MPa) within a depth of a few microns. Thus, using a polycrystalline behaviour law for indium, heterogeneities can already be seen pixel by pixel when applying thermal fields between the centre and the edge of the detector. In order to have a more precise estimation of the stress state in each pixel of the detector, other simulations were launched considering the single crystal nature of each solder bump as well as the influence of the crystallographic orientation and the anisotropic CTE of indium. The numerical results showed that the CdHgTe law was a weak impacted, but according to their crystallographic orientation, the indium solder bumps could be more in compression at 293 K and 100 K: this difference in the stress/deformation could lead to possible cracks at the interface with the CdHgTe and/or silicon layers and explain some defects such as the dead pixels appearing in the detector during elaboration and service life.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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