T-type Multilevel Inverters: A Comparative Performance Analysis

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***Abstract*—T-type multilevel inverters are a potential alternative because of their increased efficiency and low conduction losses. A conventional two-level inverter is extended with a bidirectional active switch to form a T-Type topology. There are a few T-Type MLIs formulated based on requirements and applications. This work provides a comparative analysis of three different T-Type five-level MLIs with a five-level cascaded H-Bridge converter. Four multi-carrier pulse width modulation (PWM) strategies, i.e., phase disposition PWM (PDPWM), phase opposition disposition-PWM (PODPWM), alternate phase opposition disposition-PWM (APODPWM), and Hybrid PWM schemes are implemented to evaluate the performance of these MLIs. They are operated over a wide range of modulation indices, and the converter output voltage, total harmonic distortion (THD), and characteristics are observed. MATLAB\Simulink environment is used for this comparative performance analysis.**

Keywords - Multilevel inverters, T-type converters, cascaded H-bridge (CHB), performance analysis.

I. Introduction

The demand for high-power apparatus for industrial applications has sharply risen in recent years. With features like reduced voltage stress across semiconductor switches, less common-mode voltage, and enhanced output voltage profile, multilevel power inverter structures are considered for medium to high power applications [1]. They also offer lower dv/dt per switching, operate at a lower switching frequency, and thus provide high efficiency than standard two-level inverters [2], [3]. Multilevel inverters (MLIs) also reduce the output filter size and required semiconductor switch rating, thus reducing the overall system cost and weight and increasing efficiency.

The most common MLI topologies are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge [4]. Modular multilevel, active neutral point, dual-output multilevel, and T-type multilevel converters are gaining popularity in recent years [5]–[8]. The output voltage of MLIs is regulated using pulse with modulation (PWM) techniques like space vector modulation (SVM), third harmonic injection, sinusoidal pulse-width modulation (SPWM), and selective harmonic elimination (SHE) [9], [10]. The most commonly used among these techniques is SPWM. For MLIs, the further classification of SPWM includes level-shifted pulse width modulation (LSPWM) and phase-shifted pulse width modulation (PSPWM) [11]. The sub-classes of LSPWM are In Phase Disposition (IPD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD). It is reported that IPD-LSPWM outperforms APOD-LSPWM and PSPWM in terms of line THD and performance. These PWM schemes use one sinusoidal reference signal, and the 'n' number of the carrier signals is used to operate an MLI of 'n+1' level.

For low-voltage applications, the basic three-level T-type converter $(3LT^2C)$ was introduced in [8]. This converter extends the traditional two-level design and adds an active bidirectional switch to the DC-link midpoint to improve output voltage quality. The $3LT^2C$ combines the benefits of the three-level topology with that of the two-level, providing better output quality, reduced switching, and conduction losses [12]. Due to reduced conduction losses, this architecture exhibits a high efficiency at low switching frequencies in contrast to the three-level NPC converter. Another benefit is the absence of two clamped diodes per bridge leg because of the active bidirectional switch at the DC-link midpoint. Multiple levels in the output voltage can be achieved by cascading numerous 3-level TNPCs similar to CHB-MLI. The idea behind cascading is to add 'n' 3-level inverter blocks in series to produce '2n+1' levels.

The 5-level T-type inverter architecture was put forth in [13]–[15] to reduce the number of devices. It has become quite popular for applications like grid interfacing of renewable energy sources. This architecture doesn't have enough redundant states for a fault-tolerant operation because of the reduced power switches. A modified T-type MLI with five levels is presented in [16], [17] with an additional bidirectional switch to make it fault-tolerant. [18] proposes a cascaded T-type neutral point clamped inverter (5L-CTNPC), and this power topology is analyzed for a rooftop grid-connected PV system.

The works mentioned above have presented different T-type topologies, with one or two modulation techniques and their advantages. However, these topologies are yet to be quantified and classified from the perspective of an established MLI. Hence a detailed analysis is required to evaluate the performance of these novel T-type MLIs. This work attempts to provide a detailed comparative performance analysis of three different T-type converters with CHB MLI. Three level-shifted multi-carrier PWMs and a hybrid PWM technique are utilized for this analysis. The paper is organized as follows: first, the cascaded H-bridge and T-type converter topologies are described. Second, CHB MLI is operated with different

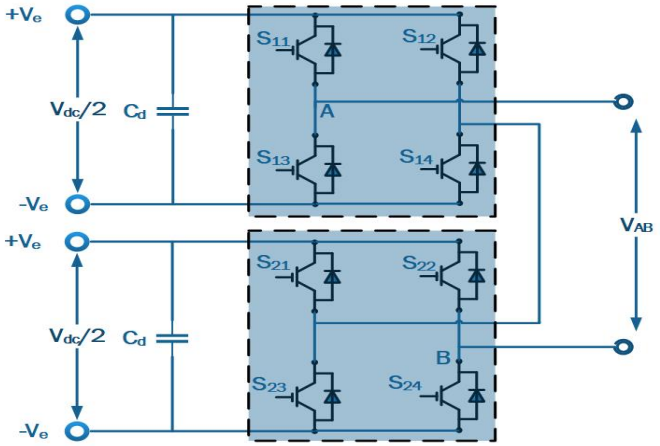

Fig. 1. Single phase 5-level CHB inverter.

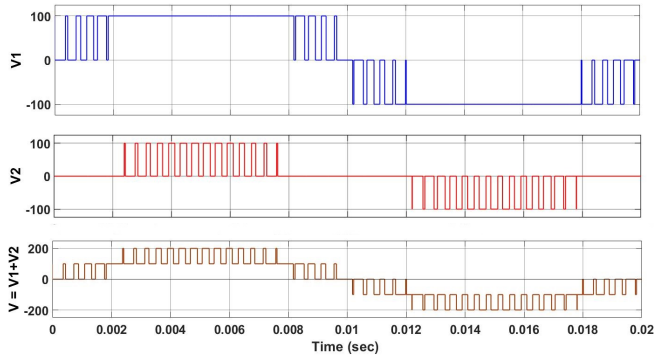

Fig. 2. Formation of 5-level output for CHB by cascading two 2-level.

multi-carrier PWM techniques and evaluated based on THD. Finally, the optimal PWM technique is applied to all three T-type MLIs and CHB, and a detailed comparative performance analysis is provided. Simulations are carried out using Matlab-SIMULINK software.

II. Cascaded H-Bridge Multilevel Inverter

Cascaded H-bridge (CHB) MLI, shown in Fig. 1 uses two series-connected single-phase full-bridge inverters with individual DC sources. Series connection improves the output voltage levels and lowers harmonic distortion. Two H-bridge output voltages are added to generate a higher-level output voltage waveform. If the magnitude of DC supplies on the input side is same for both H-bridges, then the configuration is said to be symmetrical MLI configuration, else an asymmetrical configuration. Fig. 2 depicts the output voltage generation for a five-level CHB.

A. SPWM-based modulation technique

There are different pulse width modulation (PWM) techniques available for MLIs. For a five-level CHBMLI, the reference signal is compared with four (5-1) carrier signals. If the sinusoidal reference waveform has a modulation frequency f_m with a peak amplitude A_m and the triangle carrier waveform has a peak amplitude with a frequency of A_c and f_c, respectively. Then, the amplitude modulation index and modulation frequency ratio are given as follows:

$$m_a = \frac{A_m}{A_c}, \qquad m_f = \frac{f_m}{f_c} \tag{1}$$

The use of multiple carriers in PWM falls under the following categories:

1) Phase Shift PWM (PS-PWM): Phase Shift Pulse Width Modulation (PS-PWM) is the most frequently used approach in MLIs. The carrier signals of various cells in a cascaded H-bridge multi-level inverter are phase-shifted by $180°/n$, where 'n' is the number of cells in each phase and is $90°$ for a 5-level CHB inverter. This phase-shifting process is illustrated in Fig. 3(a) with its harmonic spectra for 5-level CHB. It is easy to implement and has some benefits, such as uniform power distribution and an output current with a high-quality waveform.

2) Level Shift PWM (LS-PWM)): In the LS-PWM, all carrier signals are dispositioned vertically concerning the zero reference line while equal in amplitude, frequency, and phase. Four (5-1) carrier signals, two above and two below zero-reference lines are required for a five-level CHB inverter. The amplitude modulation index is given in equation 2; N is the number of levels in an MLI.

$$m_a = \frac{A_m}{(N-1)A_c} \tag{2}$$

The LSPWM can be sub-classified int: (a) In phase disposition (IPD); all carrier signals in this type of LSPWM) are in phase with one another, as depicted in Fig. 4(a). (b) Phase opposition disposition (POD); in this method, the carrier signals above the zero reference line are $180°$ out of phase with those signals below the zero reference line as shown in Fig. 4(b). Alternate phase opposition disposition (APOD); It is as shown in Fig. 4(c); carrier signals in this method are $180°$ out of phase with its neighbor carrier.

3) Hybrid-PWM: This PWM scheme hybridizes carrier disposition-PWM (CD PWM) and phase disposition-PWM (PD-PWM) schemes. Fig. 3(b) shows the hybrid PWM with its harmonic spectra.

TABLE I
Switching Table Tor Five-level CHB

State No.	Switching Signals								Output Voltages
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	V_{AB}
1	ON	OFF	OFF	ON	ON	OFF	OFF	ON	+Vdc
2	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	+Vdc/2
3	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
4	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	-Vdc
5	OFF	ON	ON	OFF	OFF	ON	ON	OFF	-Vdc/2

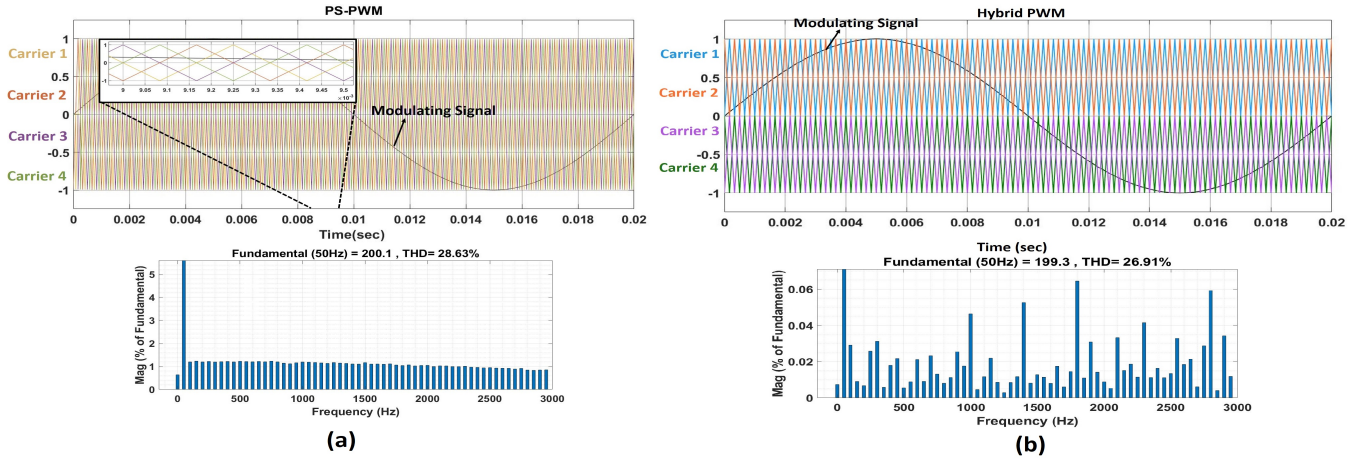

Fig. 3. (a) PS-PWM with its harmonic spectra implemented to 5-level CHB. (b) Hybrid-PWM with harmonic spectra implemented to 5-level CHB.

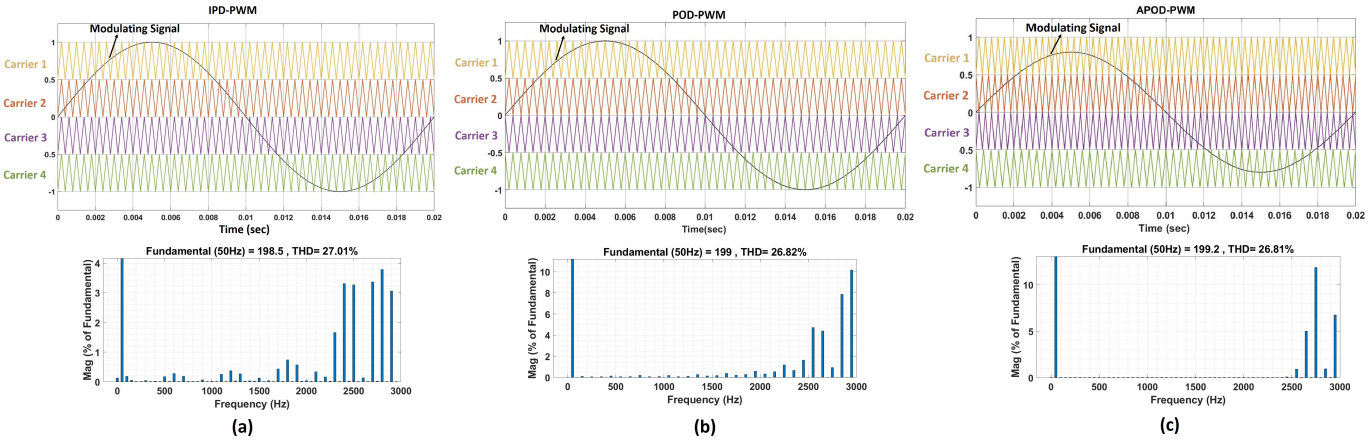

Fig. 4. (a) IPD PWM with its harmonic spectra for 5-level CHB. (b) POD PWM with its harmonic spectra for 5-level CHB. (c) APOD PWM with its harmonic spectra for 5-level CHB.

III. 5-Level T-type MLI Topologies

A. Five-Level T-Type Asymmetrical H-Bridge Converter (5L-TAHC)

It is also known for Reduce Device Count (RDC) T-type MLI, and has been reported in [13]–[15]. It has become quite popular for applications like solar (PV), flexible AC transmission systems (FACTS), multi-energy storage systems, automotive inverter systems, etc. 5L-TAHC utilizes bidirectional and unidirectional switches to form the topology. Each phase needs two dc sources or one dc source with two dc-link capacitors, one bidirectional switch (S_{13} and S_{14}), and four unidirectional switches (S_{11}, S_{12}, S_{21}, and S_{22}). Five-level of phase voltage generated by this converter is shown in Fig. 5. Considered bidirectional switch uses two unidirectional switches (S_{13} and S_{14}) connected in a common emitter configuration or common collector configuration. The requirement for bidirectional switches and capacitors increases with an increase in converter level; however, H-bridge switches remain the same. A total of [4 + (N-3)] switches are required for each phase to achieve "N" levels in phase voltage and (2N-1) levels in the line voltage. Here, "4" denotes the number of switches in an H-bridge, and the "N-3" indicates the switches used for bidirectional operation.

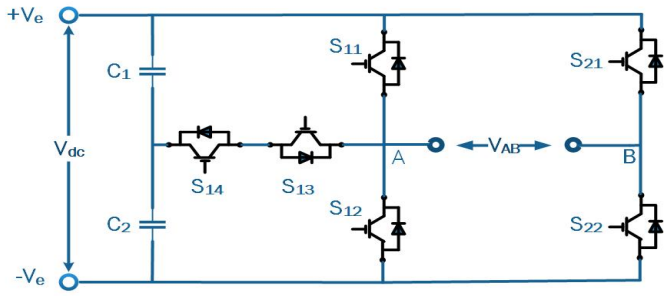

Fig. 5. 5-level-T-Type AHB inverter topology.

Table II displays switching states of 5L-TAHC to achieve appropriate voltage values per phase.

The load voltage can be represented using input voltages

TABLE II
VALID SWITCHING STATES FOR 5L-TAHC

State No.	Combination of switches	Output Voltages
1	S_{11},S_{21}	0
2	S_{12},S_{22}	0
3	S_{13},S_{22}	V_{dc}/2
4	S_{14},S_{21}	-V_{dc}/2
5	S_{11},S_{22}	V_{dc}
6	S_{21},S_{12}	-V_{dc}

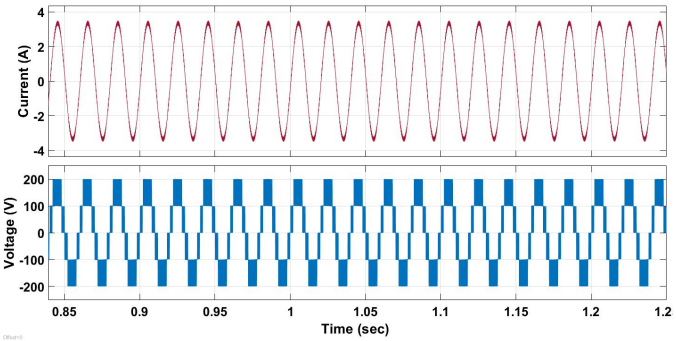

Fig. 6. 5-level-T-Type AHB inverter output voltage with load current.

and switching functions as follows:

$$V_{AB}(t) = (1 - S_{11}S_{21})(1 - S_{12}S_{22}) \\ (\frac{V_{dc}}{2}(S_{11}S_{22} - S_{14}S_{21} - S_{12}S_{21}) \\ +\frac{V_{dc}}{2}(S_{13}S_{22} + S_{11}S_{22} - S_{12}S_{21})) \quad (3)$$

Fig. 6 presents the output voltage V_{AB} and load current i_L. Fig. 7 shows the balanced capacitor voltage in 5L-TAHC.

B. Five-level Fault Tolerant T-Type Converter (5L-FTTC)

The 5L-TAHC is modified to increase the reliability and fault-tolerant (FT) ability in a converter-drive system [16], [17]. This is achieved by adding a bidirectional switch (S_{21} and S_{23}) as shown in Fig. 8. The load voltage can be expressed in terms of switching mechanisms and input voltages as follows:

$$V_{AB}(t) = (1 - S_{11}S_{21})(1 - S_{12}S_{22})(1 - S_{13}S_{14}S_{23}S_{24}) \\ (\frac{V_{dc}}{2}(S_{11}S_{22} - S_{14}S_{21} - S_{12}S_{21} + S_{11}S_{23}) \\ +\frac{V_{dc}}{2}(S_{13}S_{22} + S_{11}S_{22} - S_{12}S_{21} - S_{12}S_{24})) \quad (4)$$

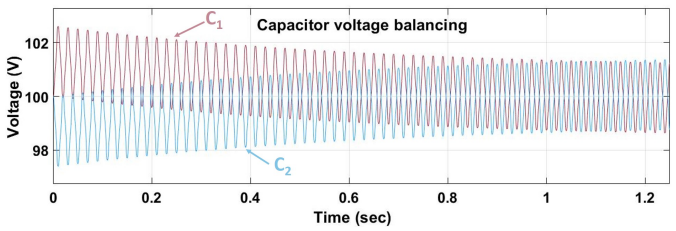

Fig. 7. Capacitor voltage balancing of 5-level-T-Type AHB inverter.

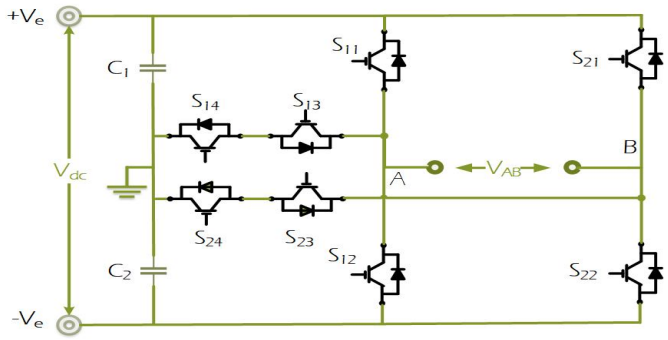

Fig. 8. 5-level FT T-Type inverter topology.

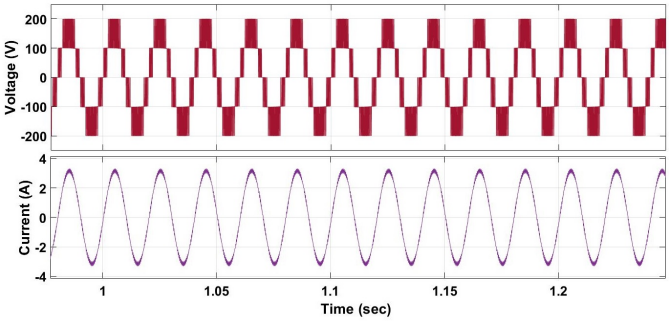

Fig. 9. 5-level FT T-type inverter output voltage with load current.

Valid switching states for 5L-FTTC using the above analysis are illustrated in Table III.

TABLE III
VALID SWITCHING STATES FOR 5-LEVEL FT T-TYPE

State No.	Combination of switches	Output Voltages
1	S_{11},S_{21}	0
2	S_{12},S_{22}	0
3	S_{13},S_{14},S_{23},S_{24}	0
4	S_{11},S_{23}	V_{dc}/2
5	S_{13},S_{22}	V_{dc}/2
6	S_{12},S_{21}	-V_{dc}/2
7	S_{24},S_{12}	-V_{dc}/2
8	S_{11},S_{22}	V_{dc}
9	S_{21},S_{12}	-V_{dc}

Fig. 9 presents the outcomes for output voltage V_{AB} and load current i_L with Fig. 10 showing the capacitor balancing of this T-type of topology.

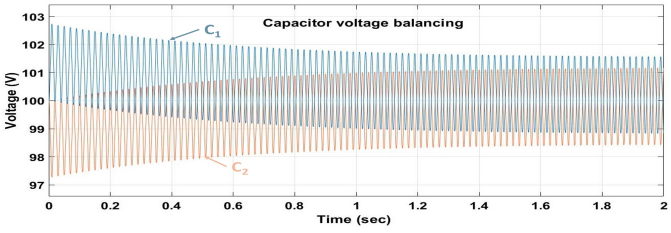

Fig. 10. Capacitor voltage balancing of 5-level FT T-type inverter.

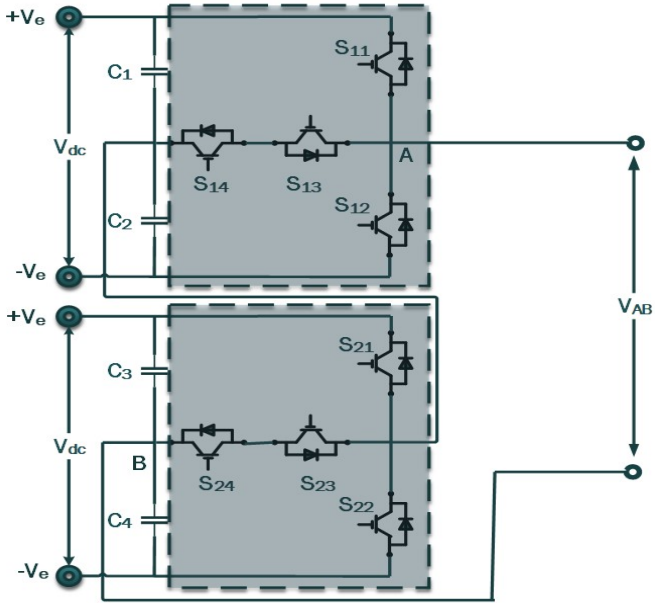

Fig. 11. 5-level CTNPC inverter topology.

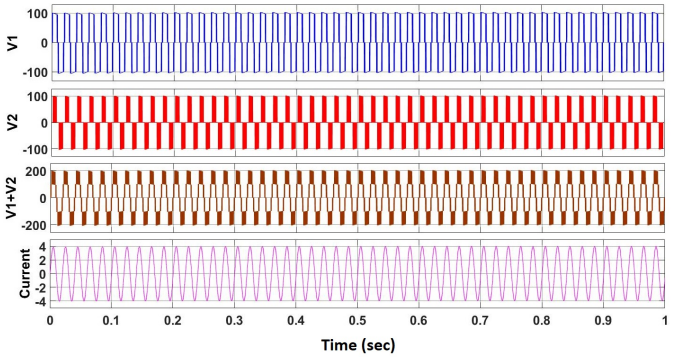

Fig. 12. 5-LCTNPC inverter output voltage with load current.

C. Five-Level Cascaded T-Type Neutral Point Clamped Converter (5L-CTNPC)

This type of topology is analyzed for a rooftop grid-connected PV system in [18]. The 5L-CTNPC configuration comprises two cascaded three-level T-Type converters $(3LT^2C)$.

The $(3LT^2C)$ provides 3-level of output voltage i.e. V_{dc}/2, 0 and -V_{dc}/2. A cascade can generate five voltage steps by connecting two $(3LT^2C)$ cells. The 5L-CTNPC topology is shown in Fig. 11.

The reference signal is compared with four carriers to generate the switching pulses for S_{11}, S_{12}, S_{21}, and S_{21}. Respective complimentary signals are provided to S_{13}, S_{14}, S_{23} , and S_{24}. Fig. 12 presents the output voltage V_{AB} and load current i_L of 5-LCTNPC, and Fig. 13 shows the balanced capacitor voltage for this topology.

The load voltage can now be expressed in terms of switching

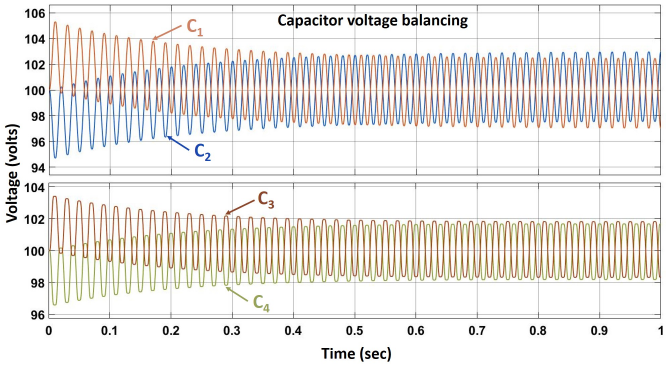

Fig. 13. Capacitor voltage balancing of 5-level CTNPC inverter.

mechanisms and input voltages as follows:

$$V_0(t) = \frac{V_{dc}}{2}(S_{11} + S_{14} - 1) + \frac{V_{dc}}{2}(S_{21} + S_{24} - 1) \quad (5)$$

From the above analysis, the valid switching states for the CTNPC inverter topology can be concluded as illustrated in Table IV.

TABLE IV
SWITCHING TABLE FOR 5L-CTNPC

State No.	Switching Signals				Output Voltages
	S_{11}	S_{14}	S_{21}	S_{24}	
1	1	1	1	1	+Vdc
2	1	1	0	1	+Vdc/2
3	0	1	1	1	+Vdc/2
4	1	1	0	0	0
5	0	0	1	1	0
6	0	1	0	1	0
7	0	1	0	0	-Vdc/2
8	0	0	0	1	-Vdc/2
9	0	0	0	0	-Vdc

The simulation results for different LS-PWM, PS-PWM, and Hybrid-PWM are shown with their harmonic spectra at the modulation index one. The design parameter considered includes a 200V dc voltage source, capacitance 2200μF resistance 50Ω, and inductance of 25mH. The comparison of different 5-level T-Type inverters with CHB is shown in table V.

TABLE V
COMPARISON OF FIVE-LEVEL CHB WITH THREE DIFFERENT FIVE-LEVEL T-TYPE TOPOLOGIES

Topology	CHB	T-Type AHB	FT T-type	CTNPC
No. of dc voltage source	2	1	1	2
No. of dc-link capacitors	2	2	2	4
No. of switches	8	4	4	4
No. of Bidirectional switches	0	1	2	2
THD (LS-PWM)	27.01	26.87	26.84	26.87

IV. CONCLUSION

This paper evaluates three different five-level T-type MLIs with a five-level cascaded H-bridge MLI and provides a

comparative performance analysis. CHB MLI is tested with four different PWM techniques, i.e., PD-PWM, POD-PWM, APOD-PWM, and Hybrid PWM, and the best suitable PWM technique is utilized for the performance analysis. MLIs are evaluated concerning the number of dc voltage sources, dc-link capacitors, switches required, total harmonic distortion (THD), and efficiency. The conclusive remarks are presented as follows:

1) 5L-TAHC and FT T-type require relatively less dc voltage sources when compared to the other two. The number of DC-link capacitors required by 5L-CHB, 5L-TAHC, and 5L-FTTC are the same. 5L-CTNPC, on the other hand, requires twice that of remaining MLIs.
2) 5L-FTTC and 5L-CTNPC uses the same number of switches as in 5L-CHB. However, with 5L-TAHC, two switches are reduced per phase, thus generally referred to as reduced switch count T-type MLI.
3) 5L-CHB provides almost the same THD when operated with three different LS, a PS, and a Hybrid PWM. T-type converters are operated with LS PWM only, and they too provide a similar THD as that of 5L-CHB MLI.
4) With the reduced number of switches, the fault tolerance of 5L-TAHC is low. 5L-CHB and 5L-CTNPC are partially fault-tolerant due to their cascaded structure. FT T-type is completely fault-tolerant and reliable compared to all other MLIs.

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